OPERATING MANUAL

SX/12 DATA CHANNEL SIMULATOR

Version 3.4a

October 23, 1992

L009-A

ADTECH™

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WARRANTY

This product is warranted against defects in materials and workmanship for a period of one year from date of shipment. Adtech will, at its options, either replace or repair the products which prove to be defective, during the warranty period.

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LIMITATION OF WARRANTY

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SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service and repair of the instrument. Failure to comply with these precautions or warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the product. Adtech assumes no liability for the operator's failure to comply with these requirements.

LIVE CIRCUIT HAZARD

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Power cable should be removed first, before removing instrument cover.

DO NOT SERVICE ALONE

Unless another person capable of rendering first aid and resuscitation is present, do not attempt servicing.

INSTRUMENT GROUNDING

To minimize shock hazard, the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three conductor power cable. This power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to the safety ground at the electrical outlet.

PARTS SUBSTITUTION OR INSTRUMENT MODIFICATIONS

Do NOT perform unauthorized modifications or parts substitution because of the possibility of introducing additional hazards. Return the instrument to Adtech for repair to ensure that safety features are maintained.

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What's New in This Version

New in This Manual, Version 3.4

This manual describes the current release of the SX/12 operating software, Rev. 3.4, which adds several new features and keys to the SX/12. These features make operation of the SX/12 more flexible and the setting up of parameters easier and quicker. The keys are added by putting additional legends on the [X 10^3] and [X 10^6] keys.

Enabling/Disabling the Error Generator

This feature permits temporarily disabling or re-enabling the error generator with a single key press. While disabled, no errors are injected regardless of error parameter settings. This is useful for doing a quick system operational check without errors to confirm proper system setup before beginning a test involving errors. It also useful for cleanly changing from one error setup to another without having unintended errors injected while the various error parameters are being changed.

If the SX/12 error generator is programmed to generate random or burst errors on the East or West channels or both, all errors can be temporarily disabled by pressing the [ERR] key in the Entry key group. While the error generator is disabled, the display changes to a blinking message indicating errors are disabled. While disabled, the error parameters can be reprogrammed using their normal parameter entry keys.

To restore errors, simply press the [ERR] key again. This returns the display to normal and re-enables the error generator with the current error parameters determining the errors to be injected.

Copying Parameters Between the East and West Channels

All SX/12 error parameters have independent settings for the East and West directions of the simulated channel. In many cases, it is normal to have the error parameters for the East and West directions of the channel set to the same values.

A new key has been added that permits all of the four error parameters (Random Error Rate, Burst Length, Gap Length, or Burst Density) to be copied from the East to West or West to East channel directions with only two keystrokes. This permits you to enter the parameters once, and then simply copy the parameters into the other channel direction.

To copy the error parameters in either direction, press the [E<->W] key. A prompting screen is displayed permitting you to select which parameters are to be copied. Press either the [1] key to copy the parameters from the East to the West direction or the [3] key to copy the parameters from the West to the East direction. When the appropriate key is pressed, the parameters are copied and you are returned to the main screen display.

New Extended T1/E1 Simulation Option

The new Extended T1/E1 Simulation Option replaces the old Extended T1 Simulation Option and now supports E1 (G.703)(2.048 Mbps) formats as well as T1. Up to ten different delays can be assigned to subchannels, many new error types are available, and it is in general much more capable than the previous option.

As of this manual, the second software revision for the new Extended T1/E1 Simulation Option is available. The new software for this option replaces version 3.3 and updates several of its features. Data bits for clear channel T1 and E1 formats now are numbered starting at one instead of zero. A bit mask has been added to channelized formats to permit enabling or disabling the individual bits in the targeted time slots to receive targeted errors. The default error targeting settings have been changed to no errors targeted and the default delay targeting settings have been changed to the delay tap corresponding to the main channel delay. These changes make the option easier to use in many applications. See Appendix K for details on the new extended T1/E1 simulation option.

Chapter 1
General Information

Introduction

This manual describes how to operate the Adtech Model SX/12 Data Channel Simulator. The three SX/12 versions, SX/12-2, SX/12-1, and SX/12-0 are referred to as SX/12 when the discussion is common to all three. This chapter describes the product and its features.

Manual Contents

This manual contains instructions and information to help you set up and operate the SX/12. It shows how to set up the data rate, delay, and error simulation parameters. It also shows how to program parameter sequences for simulating changing error conditions. In the appendices are sections that describe the SX/12 interface modules, SX/12 specifications, and IEEE-488 remote interface.

SX/12 Description

The SX/12 Data Channel Simulator creates a controlled environment for testing, tuning, or demonstrating data communications equipment. Its delay buffer and error generator simulate the major characteristics of satellite and terrestrial data channels. Delays and/or errors can be selected to assist in hardware and software performance testing, stress testing, optimization, and off-line development. Programs can be entered to simulate complex error scenarios or test sequences. The SX/12 can also be added to real data channels to insert additional delays or errors to test their effects on the on-line communications equipment.

Front Panel

The SX/12 front panel includes a power switch, a 2-line 40-character LCD display, indicators and key switches. See Figure 1.0 .

The LCD display is used to indicate the SX/12 parameters. On the left side of the display are the data rate and delay parameters. On the right side of the display are the error parameters. The top line displays the error parameters for the East channel and the bottom line displays the error parameters for the West channel. The error parameters include: random error rate, burst length, gap length, and burst density. The contrast of the LCD display can be adjusted with a 1/16 inch flat blade jeweler's screw driver through the hole provide on the upper left corner of the front panel.

Located beside the power switch is a green indicator that illuminates when power is applied. Along the right edge of the LCD display are two red indicators that flash when errors are generated on the East and West channels. The two yellow indicators located below the LCD display show the positions of the DCE/DTE switch and the external transmit timing switch, both located on the rear panel.

The key switches are arranged in four groups. These groups include numeric keys, parameter entry keys, error parameter keys, and function keys. The display and keys are discussed in detail in Chapter 3 of this manual. The numeric keys also double as edit function keys in the program edit mode. This is discussed further in Chapter 4.

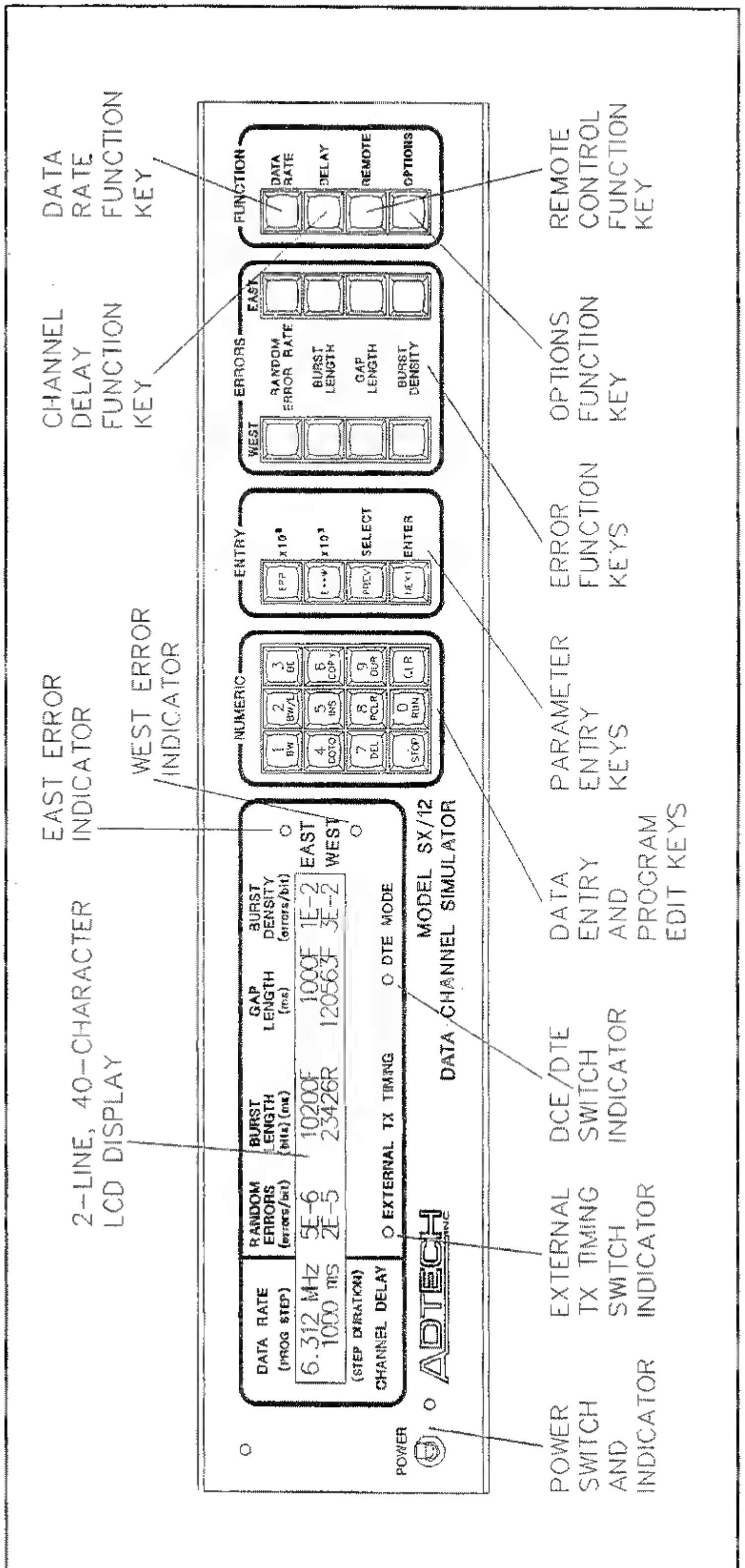

Figure 1.0 SX/12 Data Channel Simulator Front Panel

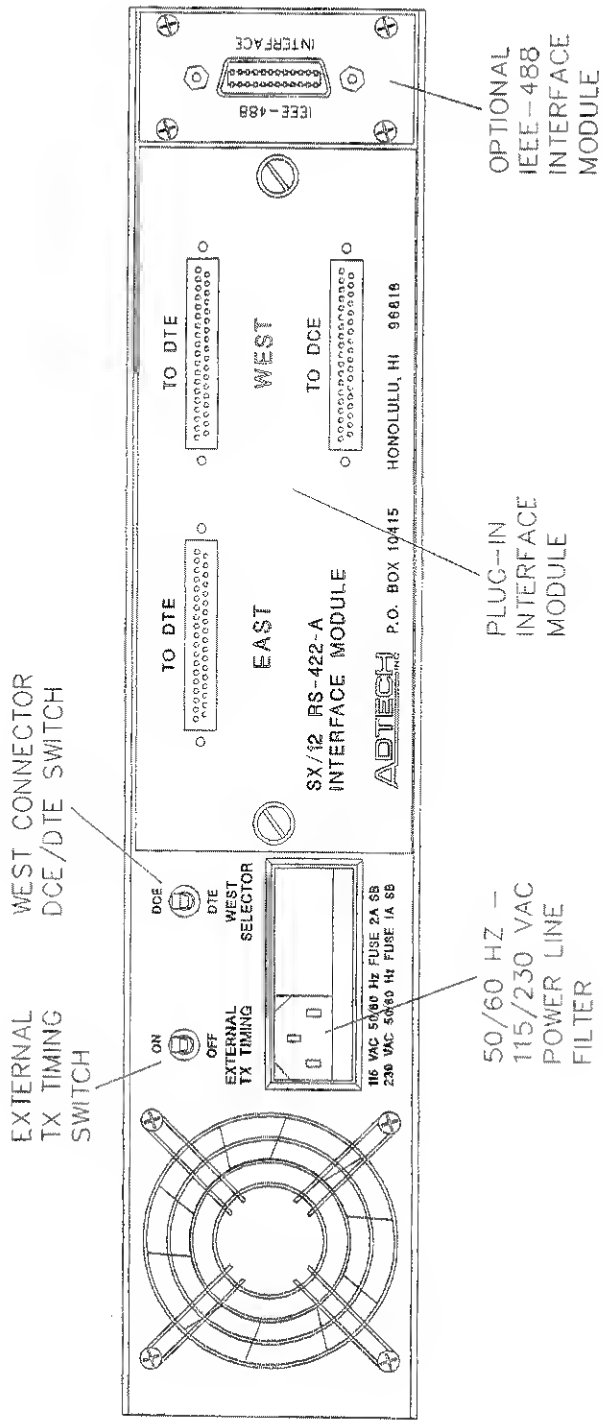

Figure 1.1 SX/12 Data Channel Simulator Rear Panel

Rear Panel

The SX/12 rear panel holds the power receptacle, cooling fan, user-plug-in interface module, optional IEEE-488 or RS-232-c remote control interface, DCE/DTE switch, and the external transmit timing switch. See Figure 1.1 .

Full-Duplex Operation

The SX/12 contains two data channels, referred to as the East and West channels. East bound data enters via the West connector, passes through the East channel, is controlled by the East parameters, and exits out of the East Connector on the plug-in interface module. West bound data enters via the East connector, passes though the West channel, is controlled by the West parameters, and exits out of the West Connector. See Figure 1.2.

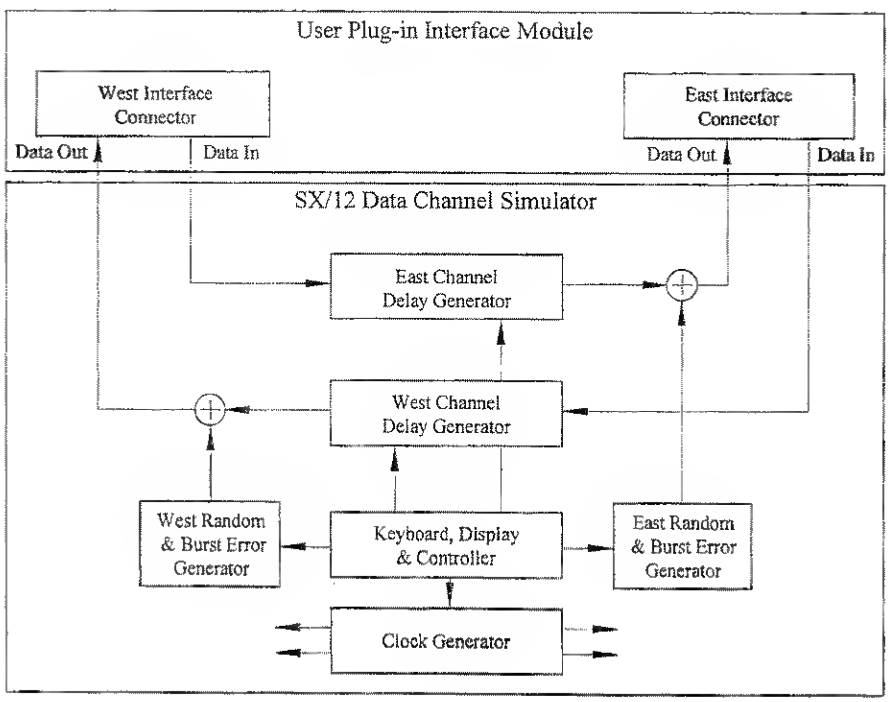

Figure 1.2 SX/12 Block Diagram

Delay Generator

The SX/12 has a variable length, first-in-first-out buffer in each channel. The length of this buffer is determined by the entered delay parameter and the rate that data passes through it. If either the delay or the data rate parameter is changed, the buffer length will be recalculated and reset. The minimum length of the buffer is 24 bits and increases in increments of 8 bits. The effect of this granularity becomes apparent at the very low data rates, (i.e., minimum delay at 100 Hz. is 240 ms. with increments of 80 ms.). If zero delay is entered, the delay

generator is bypassed to provide a true zero delay. The maximum buffer length depends on the SX/12 version. The SX/12-0, -1, and -2 has maximum buffer lengths of 65.536 bits, 2,097,152 bits and 8,388,608 bits respectively.

A single delay parameter is used to set the delay for both channels. The delay parameter determines, in milliseconds or bytes of delay, how long data takes to pass through each channel. (For example, if the delay parameter is set to 1000 ms., the data would take 1 second to pass through the East channel and 1 second to pass through the West channel.)

If an external clock is used, it is expected that the East and West channels will have the same nominal data rate. The data rate parameter must be set to the nominal data rate used so that the proper buffer length will be determined by the SX/12.

Error Generator

The SX/12 contains an error generator that has four bit-error sources with error rates that can range from 1 x 10^{-9} to as high as 1 error/bit. Two of the bit-error sources are used to inject random errors into each channel. The other two bit-error sources are used to generate burst errors for each channel.

The random error rates are individually set for the East and West channels. Both the mantissa and the exponent of the error rate are entered. An exponent of zero gives an error rate of 1 error/bit. A mantissa of zero turns off the random errors. Random errors begin immediately after the random error rate has been entered. It is used mainly to simulate background errors caused by Gaussian noise.

The East and West burst error generators are independently controlled by their own burst density, burst length and gap length parameters. The burst length parameter controls the duration of the error burst. The first and last bits of the error burst always generate an error in the data stream. The error rate of the remaining bits in the burst is controlled by the burst density parameter. The time interval between error bursts is determined by the burst gap length parameter. Burst errors are used to simulate periodic and sporadic bursts of errors that can occur in a data channel. See Figure 1.3 .

The burst density is entered by entering the mantissa and the exponent of the burst density. An exponent of zero gives an error rate of 1 error/bit. A mantissa of zero turns off the burst bit-error source and results in errors at only the first and last bit positions of the burst. For burst lengths of 2 or less, the burst density has no effect since it controls the error rate of the bits <u>between</u> the first and last bit positions only.

The burst length, when specified in bits, ranges from 1 to 16,777,215 bits. When specified in ms., it can range from 1 to 9,999 ms. In the fixed mode, the burst lengths are constant, equal to the burst length parameter. In the random mode, the burst lengths vary about a mean specified by the burst length parameter. (See appendix B for more details.) Setting the burst length to zero turns off the burst generator.

The gap length is specified in milliseconds and ranges from 1 to 99,999,999 milliseconds. (For the very low data rates, the minimum gap ranges from 1 to 40 milliseconds.) In the fixed mode, the gap time intervals are constant, equal to the gap length parameter. In the random mode, the gap lengths vary about a mean specified by the gap length parameter. (See appendix B for more details.) Setting the gap length to zero enters the manual burst trigger mode and allows error bursts to be triggered by pressing one of three keys on the front panel. The [1] key is pressed to trigger an error burst in the West channel. The [3] key is pressed to trigger an error burst in the East channel. Pressing the [2] key triggers error bursts in both channels. The burst error characteristics in this mode are determined by the burst density and length parameters.

The error generator can be enabled or disabled by pressing the [ERR] key in the parameter entry group. When disabled, the display will flash a message in the error parameter display area indicating that errors are disabled.

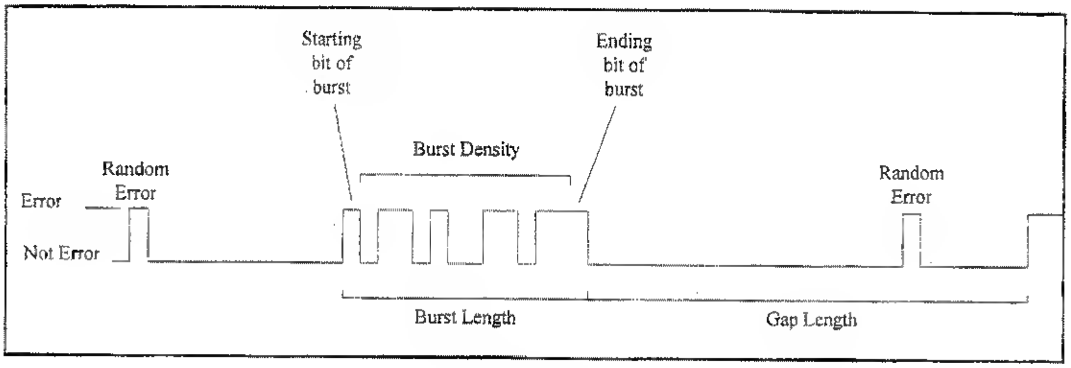

Figure 1.3

The error parameters can be reprogrammed while errors are disabled. When the error generator is re-enabled, the new error parameters take effect.

The error parameters for the East or West channels can also be copied to the other channel when both channels are to have the same error parameters. This is done using the [E<->W] key in the parameter entry group. Once the key is pressed, the display will prompt for the desired copy direction. When the direction is selected, all of the error parameters for one channel are copied to the other channel.

Data Clock Generator

The SX/12 is capable of generating a wide range of clock rates. Clock rates below 500 kHz are programmed to the nearest 100 Hz. Clock rates below 3 MHz are programmed to the nearest 500 Hz. Clock rates 3 MHz and above are programmed to the nearest 1 kHz. A single data rate parameter is entered to set the clock rate for both the East and West channels. The clock generator is based on a crystal oscillator with an accuracy and stability of25 ppm over the operating temperature range of 0 to 70°C. For applications where a higher accuracy or stability is required, the external timing options should be used.

The maximum clock rate of the SX/12 depends on the model. The SX/12-2 has a maximum clock rate of 8.448 Mb/s. The SX/12-1 has a maximum clock rate of 2.048 Mb/s. The SX/12-0 has a maximum clock rate of 100 Kb/s.

DCE / DTE and External Transmit Timing Options

The SX/12 has several configuration options built in to simplify equipment hookup. The plug-in interface module on the SX/12's rear panel contains three connectors: an East "to DTE" connector, a West "to DTE" connector and a West "to DCE" connector. The East connector is always connected to a Data Terminal Equipment. If the SX/12 is simulating a data link between two Data Terminal Equipments, the West "to DTE" connector is used. If the SX/12 is simulating a data link between a Data Terminal Equipment and a Data Communications Equipment, the WEST "to DCE" connector is used. The DCE/DTE switch on the rear panel determines which West connector is in use.

Also on the rear panel is the external transmit timing switch. This switch allows a DTE to provide its own transmit clock. When this option is used, the nominal rate of the external clock should be entered as the data rate in order for the SX/12 to operate properly. The SX/12 checks for any discrepancies between the entered data rate and the actual data rate measured on the East channel. If a discrepancy is found, a blinking data rate display occurs.

Battery-backed Setups

The SX/12 contains a button-type lithium battery that is used to retain the SX/12 parameters and program in memory. The validity of the parameters are checked on power-up and used to restore the SX/12 to its previous setup. If the parameter memory fails its check, the default parameters will be used. The default parameters are:

Data Rate: 100 Hz
Delay: 0 ms
Random Errors: 0
Burst Densities: 0
Burst Lengths: 0
Gap Lengths: Manual

Interface Signaling Lines

The RTS, CTS, DSR, DTR signaling lines at the interface are normally handled locally at the interface connectors (i.e., RTS connected to CTS, DSR forced on). The exception occurs when the delay parameter is set to zero, and the SX/12 is configured for connection to a DTE and DCE. In this case, the four signaling lines are connected between the East and West connectors, allowing the signaling information to pass through. See the appendices on the individual interfaces for more details.

Keyboard Lockout

The keyboard on the SX/12's front panel can be disabled by putting the SX/12 into the keyboard lockout mode. This feature is used to prevent accidental modification to the SX/12 parameters and program once the unit has been setup. Manual triggering of the burst errors and program execution are not affected by the keyboard lockout. This mode is indicated by the letters "KL" displayed on the lower left corner of the LCD display. See Chapter 3 for more details.

SX/12 Bypass

The SX/12 can be put into a bypass mode. When this mode is selected, the error generator and delay buffer are bypassed. All data, clock, and control signals pass through the SX/12 and experience only the propagation delay of the interface. This mode is indicated by the letters "BP" displayed on the lower left corner of the LCD display. See Figure 1.4 .

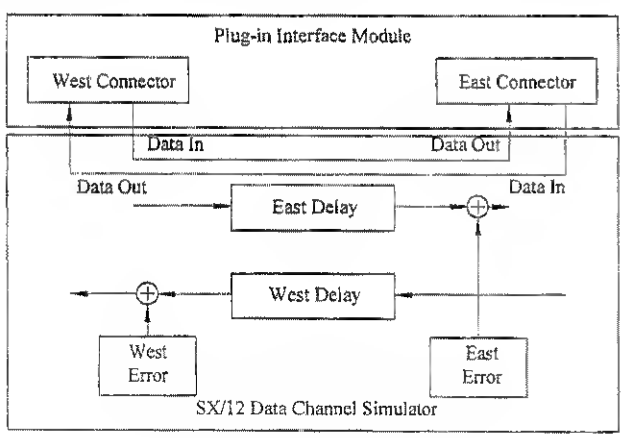

Figure 1.4 SX/12 Bypass Mode

SX/12 Loopback

The SX/12 can be put into one of two loopback modes: inward and outward loopback. When outward loopback is selected, the data is looped through the interface only and returned to the originating port. Only the propagation delay of the interface is experienced. This mode is indicated by the letters "OL" displayed on the lower left corner of the LCD display. See Figure 1.5 .

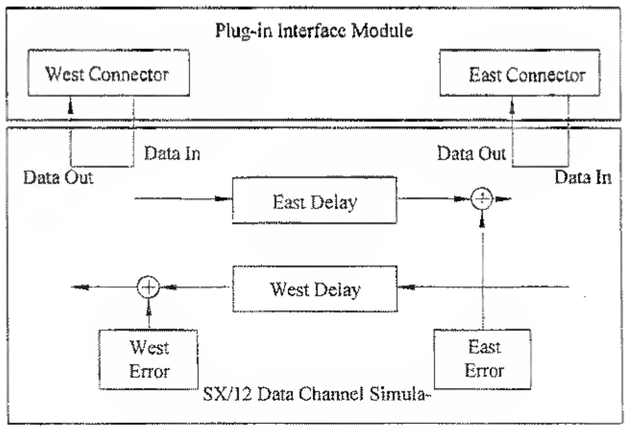

Figure 1.5 SX/12 Outward Loopback

If inward loopback is selected, the data is passed through the delay and error generator before returning to the originating port. This mode is indicated by the letters "IL" displayed on the lower left corner of the LCD display. See Figure 1.6 .

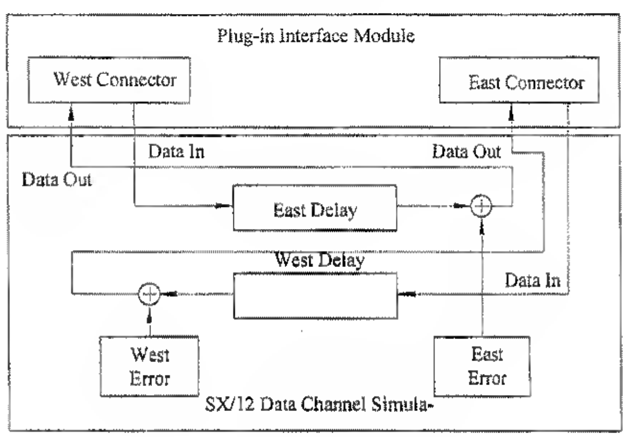

Figure 1.6 SX/12 Inward Loopback

SX/12 ASYNCHRONOUS MODE

The SX/12 asynchronous mode allows the SX/12 to be used with asynchronous data. This is accomplished by operating the SX/12 in its internal clock mode and at a rate that is 10 times the baud rate of the data. Jitter caused by the 10 times oversampling will be at worst, 10% of the data bit. The unit of the SX/12 data rate in this mode is baud and is abbreviated "bd" in the parameter display. (In the synchronous mode, the unit is Hz).

For example, if the data rate parameter is set to 9600 baud, the internal clock of the SX/12 will automatically be adjusted to 96,000 Hz. Setting a burst length of 1000 bits will caused the SX/12 to setup the hardware for 10,000 bits in order to compensate for the 10 times faster clock rate.

The asynchronous mode is set via the [OPTIONS] key and is remembered when the unit is powered down. An "asynchronous mode" message is displayed during power-up if the unit is set to be operated in that mode.

Chapter 2
Installation

Introduction

This chapter describes the installation procedures for the SX/12 Data Channel Simulator.

Installation

The SX/12 Data Channel Simulator is designed to be a bench or rack-mounted unit. If rack-mounted, a 19 inch rack is required. The rack mounting brackets are supplied with the unit.

The unit is forced air cooled by a fan located on the rear panel. The fan and the vents on the top and bottom covers should not be blocked.

Setting the Line Voltage

The SX/12 can operate from a 115 or 230 VAC, 48 to 66 Hz power source. Only the line voltage needs to be selected. The operating voltage of the SX/12 is factory set to 115 VAC. If 230 VAC is required, perform the following operation:

1. Remove the power cord from the power receptacle on the rear panel.

2. Slide the transparent door on the receptacle to the left and pull out the circuit board located beneath the fuse using a metal hook.

3. Flip the board over so that the "220" marking is right side up and re-insert the board. The "220" marking should be visible after the board has been inserted.

4. Replace the two amp fuse with a one amp fuse.

5. Re-connect the power cord.

When switching back to 115 VAC, perform the same operation as above except that the "120" marking should be visible after the board has been installed and an one amp fuse should be used.

Initial Check Out

The SX/12 unit is thoroughly tested at the factory before it is shipped. To make sure that it was not damaged in the shipping process, it should be put though its self-test.

Power up the SX/12. An initial check is performed automatically after power up. If this check is passed, the parameter display should appear. If an error message is displayed instead, contact the factory for assistance.

To initiate the self test, press the [OPTIONS] key until the 'self test' prompt appears. Then press the [ENTER] key to begin the self test. It is not necessary to have an interface module installed to run the self test. If the

self test is passed, the SX/12 will return to its parameter display. If self test does indicate a problem, call the factory for assistance. NOTE: The self test will take approximately 20 minutes to complete.

Installing the Interface Module

The SX/12 requires that an interface module be installed on its rear panel before it can be used. The following describes the procedure for installing or changing the interface module.

1. Shut off power to the SX/12. Damage could occur to the interface module and the SX/12 mainframe if installation is attempted with the unit powered up.

2. Remove the existing interface module (if any) by unscrewing the thumb screws located on its sides. Carefully pull out the module while making sure that the module's circuit board clears the rear panel opening. Remove the interconnecting cable on the module by using the ejectors on the connector. The cable should not be disconnected from the mainframe because of the difficulty in properly re-connecting it.

3. Certain interface modules have jumper and switch options that can be selected. These options should be selected before installing an interface module. See the appendices on the individual interface modules for information on the option settings.

4. To install an interface module, connect the module to the interconnecting cable by holding the module right side up in one hand. With the other hand, align the cable connector to the connector on the module and press it into place. Both connectors have a 'triangle' mark indicating pin 1 which should line up. CAUTION: Installing the cable backwards could damage both the interface module and the mainframe circuitry. Carefully insert the module into the rear panel opening, making sure that the circuit board clears the opening. Align and screw the module in place with the thumb screws.

This completes the interface module installation procedure.

Connecting the SX/12 to Two DTE's

When the SX/12 is used to simulate the data link between two Data Terminal Equipments, the West "to DTE" and the East "to DTE" connectors should be used on the interface module. The DCE/DTE switch should be switched to the DTE position.

The external transmit clock switch should be in the "off" position if the SX/12 is to provide both transmit and receive clocks for the East and West connectors. See Figure 2.0a .

The external transmit clock switch should be in the "on" position if the Data Terminal Equipments provide their own transmit clock signal. The external transmit clock received at the East connector becomes the receive clock at the West connector and vice-versa. An SX/12 generated clock is available on the transmit clock signal of the East and West "to DTE" connectors. See Figure2.0b

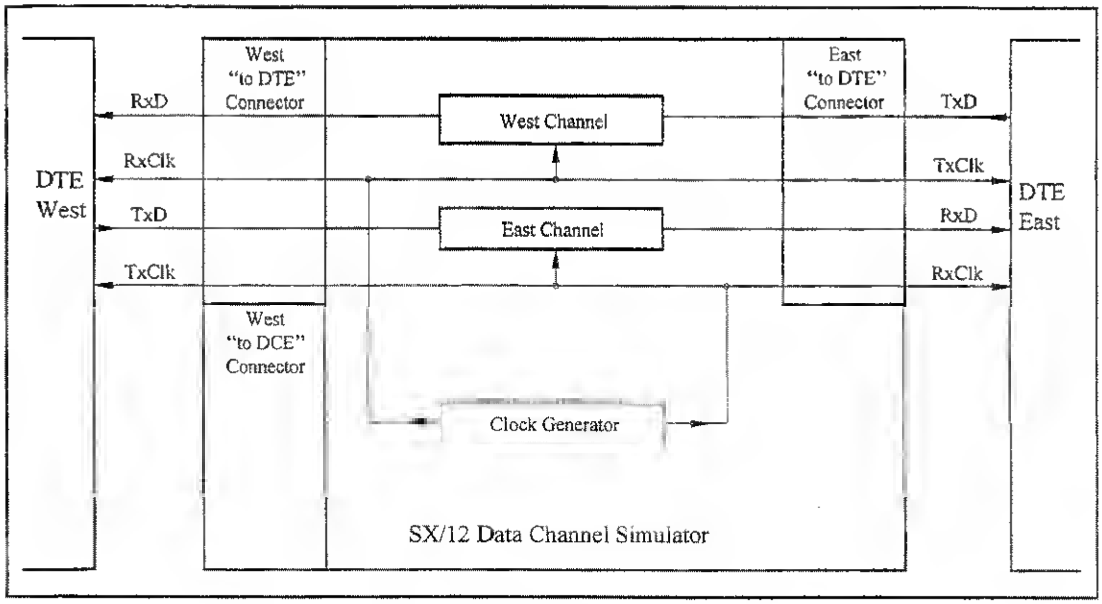

Figure 2.0a Connecting the SX/12 to two DTEs External transmit timing off, DTE selected

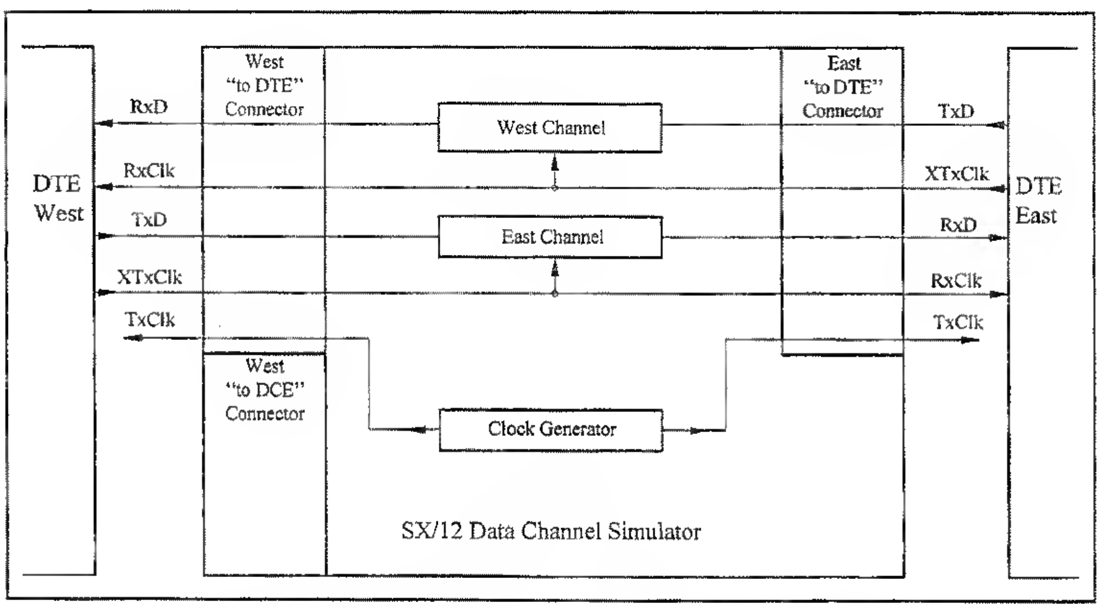

Figure 2.0b Connecting the SX/12 to two DTEs External transmit timing on, DTE selected

Connecting the SX/12 to a DTE and a DCE

When the SX/12 is used to simulate the data link between a Data Terminal Equipment and a Data Communications Equipment, the East "to DTE" connector must be connected to the Data Terminal Equipment. The West "to DCE" connector is connected to the Data Communications Equipment and the DCE/DTE switch should be switched to the DCE position.

The external transmit clock switch should be in the "off" position if the Data Communications Equipment provides the receive and transmit clocks. The SX/12 generated clock is available on the transmit clock signal of the West "to DTE" connector and also on the external transmit clock signal of the West "to DCE" connector. See Figure 2.1a.

The external transmit clock switch should be in the "on" position if the Data Terminal Equipment provides its own transmit clock signal. The SX/12 generated clock is available on the transmit clock signal of the West "to DTE" connector. See Figure 2.1b.

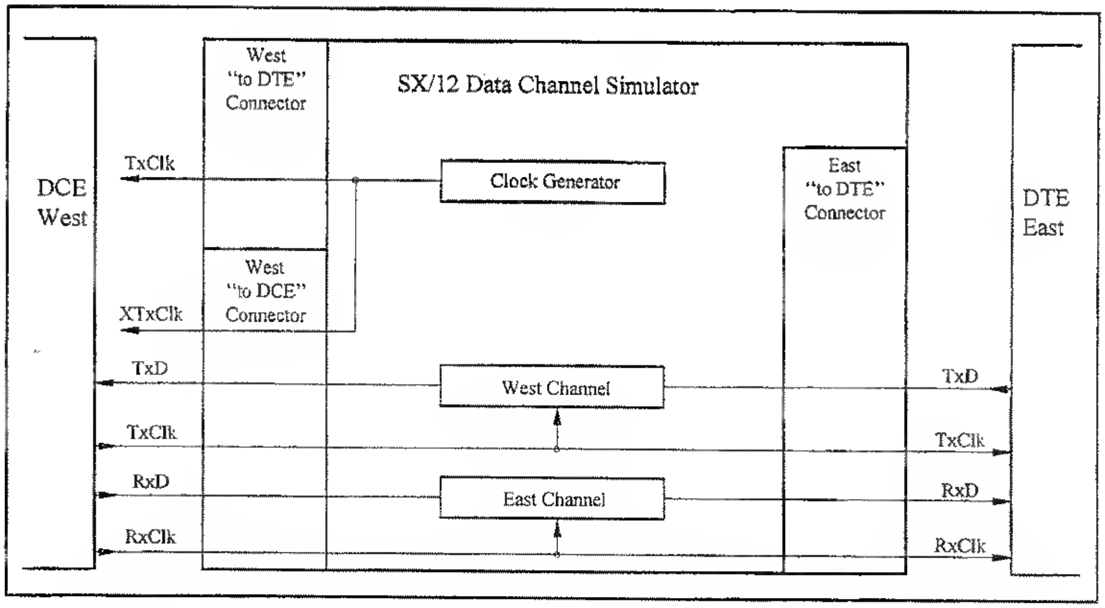

Figure 2.1a Connecting the SX/12 to a DCE and a DTE External transmit timing off, DCE selected

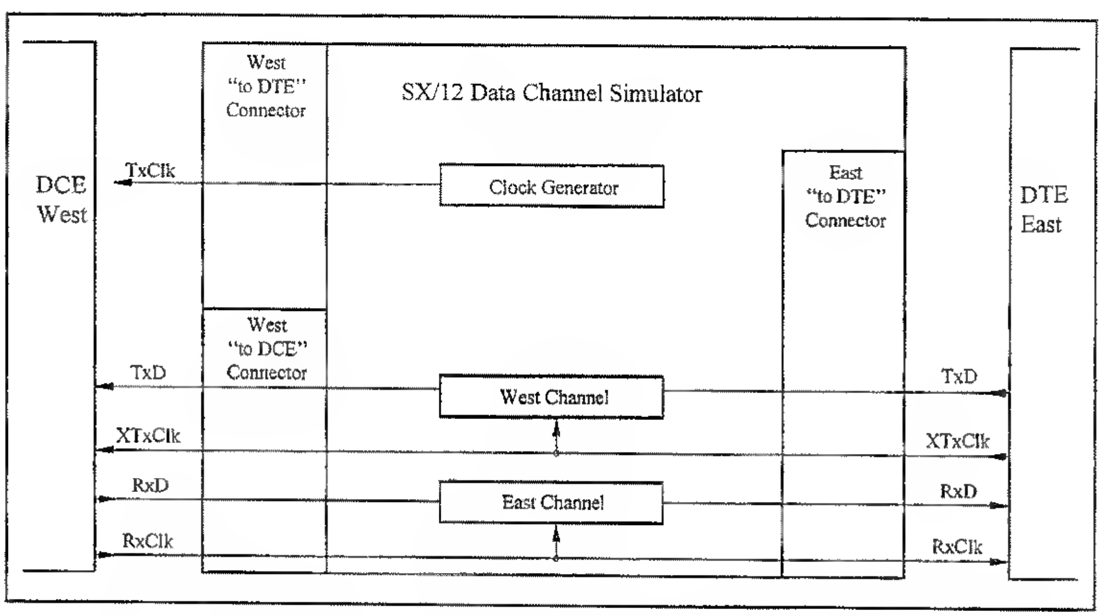

Figure 2.1b Connecting the SX/12 to a DCE and a DTE External transmit timing on, DCE selected

Chapter 3
Operation

Introduction

This chapter describes how to set the various parameters of the SX/12. It describes how to set up the SX/12 for delay and/or error generation, and also how to use the SX/12 in asynchronous applications.

SX/12 LCD Display

The LCD display is normally used to show parameter settings, but changes when functions are entered to prompts for parameter entry. Upon completion of the parameter entry, the display returns back to its normal parameter display. The following describes the fields of the parameter display.

Data Rate Field

The leftmost parameter field on the top line of the display shows the data rate that the SX/12 is set to operate at. In the synchronous, or normal mode, the data rate units are Hz, kHz, or MHz. In the asynchronous mode, the data rate unit is baud, abbreviated bd or kbd. A blinking data rate display indicates that the measured data rate does not agree with the data rate that was entered. (It is normal for the data rate display to blink for a few seconds after a new data rate parameter has been entered.) A "*" following the data rate indicates that no clock signal is present.

SX/12 Mode Field

The two leftmost character positions of the bottom line of the display show the SX/12 mode. The modes are displayed as follows:

" "	Normal mode.
"KL"	Keyboard lockout mode
"IL"	Inward loopback mode
"OL"	Outward loopback mode
"BP"	Bypass mode
"T1"	Extended T1 Simulation mode (hardware option)

Channel Delay Field

To the right of the mode display is the channel delay parameter. The units for this parameter are selectable and denoted as follows:

"ms"	Delay measured in ms.
"by"	Delay measured in bytes.

Error Parameter Fields

To the right of the data rate field are the error parameters of the East channel. Directly below them are the error parameters of the West channel.

Random Errors Field

The first field in each group is the random error parameter. The units for this parameter are errors per bit. Four characters are displayed. The first digit is the mantissa of the error rate, the next two characters are "E-", and the last character is the exponent of the error rate.

Burst Length Field

Next is the burst length parameter. Up to 8 digits are displayed, followed by units, which are selectable. They are denoted as follows:

"bF"	Fixed burst lengths measured in bits.
"bR"	Random burst lengths measured in bits.
"msF"	Fixed burst lengths measured in ms.
"msR"	Random burst lengths measured in ms.

Gap Length Field

Following the burst length parameter is the gap length parameter. Up to 8 digits are displayed, followed by units, which are selectable. They are denoted as follows:

"F"	Fixed gap lengths measured in ms.
"R"	Random gap lengths measured in ms.

Burst Density Field

The last parameter of the group is the burst density parameter. The units for this parameter are errors per bit. Four characters are displayed. The first digit is the mantissa of the burst density, the next two characters are "E-", and the last character is the exponent of the burst density.

Setting the SX/12 Parameters

The SX/12 parameters are programmed by pressing the desired parameter function key. The display changes to show the current parameter setting and a key option menu. The parameter is changed by entering a new value using the numeric keys, and entered with the [ENTER] key. The current parameter can be left unchanged by pressing the [CLR] or [ENTER] key. Erroneous entries are cleared using the [CLR] key. Out of range entries causes the parameter to be set to its limit. The setting of the individual parameters is described below.

Setting the Data Rate Parameter

1. Press the [DATA RATE] key. The first line of the display will show the current data rate setting and the measured East channel data rate.

2. Enter the desired data rate using the numeric and decimal point keys.

3. Press the [x 10^6], [x 10^3] or [ENTER] key to finish the data rate entry. If a limit is exceeded, a warning message will appear on the second line and the data rate will be set to the minimum or maximum rate allowed. After entry, the data rate is rounded to the nearest allowable rate. The display will momentarily show the entered data rate and the recalculated channel delay. If the new data rate causes other parameters to exceed their limits, they are automatically set to their respective limits.

The data rate parameter must still be set if external clocks are used. This allows the SX/12 to determine the proper buffer length needed to generate the delay displayed. The data rate display will blink if the entered data rate does not match the measured data rate of the East channel. If no clock is present on the East channel, an '*' will appear next to the data rate display.

Setting the Delay Parameter

1. Press the [DELAY] key. The first line of the display will show the current delay setting.
2. Enter the desired delay using the numeric keys, decimal point key and the [x 10^3] key if needed.
3. Press the [SELECT] key to choose between the ms. and byte delay options.
4. Press the [ENTER] key to finish the delay entry. If a limit is exceeded, a warning message will appear on the second line and the delay will be set to the minimum or maximum delay allowed. After entry, the delay is rounded to the nearest allowable delay determined by current data rate parameter.

Setting the Random Error Rate Parameters

The random error parameters for the SX/12 are set by the East and West [RANDOM ERROR RATE] keys. The East [RANDOM ERROR RATE] key sets the random error rate for the East channel. Similarly, the West [RANDOM ERROR RATE] key sets the random error rate for the West channel.

1. Press the [RANDOM ERROR RATE] key for the desired channel. The first line of the display will show the current random error rate setting.
2. Enter the mantissa of the error rate using the numeric keys. (Enter zero for no random errors.)
3. Press the [ENTER] key. The cursor will move to the exponent. (If zero was entered, this will conclude the random error rate entry.)
4. Enter the exponent of the error rate using the numeric keys. (Enter a zero if an error rate of 1 error/bit is desired.)
5. Press the [ENTER] key to conclude the random error rate entry.

Setting the Burst Error Parameters

The burst error parameters for the SX/12 are set by the East and West [BURST DENSITY], [BURST LENGTH], and [GAP LENGTH] keys. Each group of keys sets the burst characteristics for its respective channel.

Setting the Burst Density

1. Press the [BURST DENSITY] key for the desired channel. The first line of the display will show the current burst density setting.
2. Enter the mantissa of the burst density using the numeric keys.

3. Press the [ENTER] key. The cursor will move to the exponent. (If zero was entered, this will conclude the burst density entry.) NOTE: Setting the burst density to zero will not turn the burst generator off.

4. Enter the exponent of the error rate using the numeric keys. (Enter a zero if an error rate of 1 error/bit is desired.)

5. Press the [ENTER] key to conclude the burst density entry.

Setting the Burst Length

1. Press the [BURST LENGTH] key for the desired channel. The first line of the display will show the current burst length setting.

2. Enter the new burst length using the numeric , decimal point, [x 10^6], and [x 10^3] keys. Enter zero to turn off the burst error generator.

3. Use the [SELECT] key to choose between burst lengths measured in bits, fixed or random lengths, and burst lengths measured in milliseconds, fixed or random lengths.

4. Press the [ENTER] key to conclude the burst length entry. If a limit is exceeded, a warning message will be displayed on the bottom line and the burst length will be set to the minimum or maximum allowed.

Setting the Gap Length

1. Press the [GAP LENGTH] key for the desired channel. The first line of the display will show the current gap length setting.

2. Enter the new gap length using the numeric, decimal point, [x 10^6], and [x 10^3] keys. The gap length is measured in milliseconds. Enter zero if manual burst triggering is desired.

3. Use the [SELECT] key to choose between the fixed and random modes.

4. Press the [ENTER] key to conclude the gap length entry. If a limit is exceeded, a warning message is displayed and the gap length is set to the minimum or maximum length allowed.

Manual Burst Error Triggering

1. Set the burst density and burst length for the channel(s) desired as described above.

2. Set the gap length of the desired channel(s) to zero to enter the manual burst trigger mode.

3. The parameter display will now show "MANUAL" as the gap length parameter for the channel(s) involved.

4. Press the [BW(1)] key to trigger a burst on the West channel if it is set for manual triggering. Press the [BE(3)] key to trigger a burst on the East channel if it is set for manual triggering. Press the [BW/E(2)] key to trigger a burst in both channels if they are both set for manual triggering.

Other SX/12 Operations

Disabling/Enabling Errors

The SX/12 can have its error generator disabled or re-enabled with a single key press. This permits quick system checks with errors removed as well as changing from one set of error parameters to another without any intermediate error conditions occurring while the error parameters are being changed.

1. Press the [ERR] key to disable errors. A blinking message appears in the error parameter display area to warn you that errors are disabled. Pressing the [ERR] key again re-enables the current error parameters and removes the blinking message.

Copying Error Parameters Between East and West Directions

All of the programmed error parameters for the East or West channel directions can be copied to the other channel direction when both channels are to inject the same error characteristics.

1. Press the [E<->W] key to copy error parameters. A new screen appears to select the channel direction to copy to. The [1] key copies from the East to the West direction, while the [3] key copies from the West to the East direction. Once the copy direction is selected by pressing the appropriate key, the error parameters are immediately copied to the selected channel direction. The new error parameters take effect immediately.

Entering the SX/12 Program Edit Mode

The program edit mode allows parameter sequences to be entered (up to 99 steps) or edited. The program is then run from the edit mode or the normal mode.

1. Press the [OPTIONS] key until the program edit prompt appears.

2. Press the [ENTER] key to enter the program edit mode. The display will momentarily display the following prompt:
   "Press <ENTER> to step forward / Press <SELECT> to step backward"
   and then alternate the normal display with the "EDIT" display. See Chapter 4 for more details.

3. To exit the program edit mode, repeat the steps above.

Entering the SX/12 Keyboard Lockout Mode

The keyboard lockout mode allows the front panel keys to be disabled to prevent accidental changes to the SX/12 parameters. The manual burst triggering and program execution is not affected by the lockout.

1. Press the [OPTIONS] key until the keyboard lockout prompt appears.

2. Press the [ENTER] key to enter the lockout mode. The display will return to the normal parameter display with "KL" displayed in the lower left corner.

3. To exit the keyboard lockout mode, repeat the steps above.

Entering the SX/12 Bypass Mode

The bypass mode allows data in each channel to bypass the error generator and the delay buffer. No delay or errors are experienced regardless of the parameter settings.

1. Press the [OPTIONS] key until the bypass prompt appears.

2. Press the [ENTER] key to enter the bypass mode. The display will return to the normal parameter display with "BP" displayed in the lower left corner.

3. To leave the bypass mode, repeat the steps above.

Entering the SX/12 Outward Loopback Mode

The outward loopback mode allows data in each channel to bypass the error and delay generator and return to the originating port. No delay or errors are experienced regardless of the parameter settings.

1. Press the [OPTIONS] key until the outward loopback prompt appears.

2. Press the [ENTER] key to enter the outward loopback mode. The display will return to the normal parameter display with "OL" displayed in the lower left corner.

3. To leave the outward loopback mode, repeat the steps above.

Entering the SX/12 Inward Loopback Mode

The inward loopback mode allows data in each channel to pass through its error and delay generator and return to the originating port. The delay and errors experienced are determined by the delay and error parameter settings.

1. Press the [OPTIONS] key until the inward loopback prompt appears.

2. Press the [ENTER] key to enter the inward loopback mode. The display will return to the normal parameter display with "IL" displayed in the lower left corner.

3. To leave the inward loopback mode, repeat the steps above.

Entering the SX/12 Self Test

The SX/12 self test can test approximately 90% of its internal hardware including its delay buffers, error generators, burst counters and the CPU code and data memory. The test takes 20 minutes and returns to the parameter display upon completion. The SX/12 program and parameters are not destroyed by the self test.

1. Press the [OPTIONS] key until the self test prompt appears.

2. Press the [ENTER] key to begin the self test.

Simulating Only Channel Delays

If only channel delays are needed, perform the following operation:

1a. Turn off the random errors by setting the random error rate parameter for the East and West channels to zero. Turn off the burst errors by setting the burst length parameter for the East and West channels to zero.

— OR —

1b. Disable errors by pressing the [ERR] key. The errors can be restored by pressing the [ERR] key again.

3. Set the data rate parameter to the required data rate.

4. Set the delay parameter to the desired delay.

Simulating Only Channel Errors

If only channel errors are needed, perform the following operation:

1. Set the delay parameter to zero.
2. Set the data rate parameter to the required data rate.
3. Set the East and West random error rate parameters.
4. Set the East and West burst error parameters.

Using the SX/12 in Asynchronous Applications

To use the SX/12 with asynchronous data channels, set the SX/12 to its asynchronous mode as follows: (These steps should be skipped if the SX/12 is already in the asynchronous mode indicated by "bd" after the data rate).

1. Press the [OPTIONS] key until the "Enter asynchronous mode?" prompt is displayed.
2. Press the [ENTER] key to enter the mode.
3. To leave the asynchronous mode, repeat the above steps. At the "Enter synchronous mode?" prompt, press the [ENTER] key.

Connecting the SX/12 between two Data Terminal Equipments.

1. Connect the Data Terminal Equipments to the East and West "to DTE" connectors on the interface module.
2. Set the DCE/DTE switch to the "DTE" position.
3. Set the external transmit timing switch to the "off" position.
4. Set the data rate parameter to the baud rate of the asynchronous data.
5. Set the delay parameter to the desired delay.

6. Set the random error rate for each channel as described in the previous sections.

7. If burst errors are needed, set the burst length, gap length, and burst density as described in the previous sections.

Connecting the SX/12 between a Data Terminal Equipment and a Data Communications Equipment.

1. Connect the Data Terminal Equipment to the East "to DTE" connector on the interface module.

2. Using a break-out box or a modified cable on the West "to DCE" connector, connect the external transmit clock signal to the transmit and receive clock signals as shown in Figure 3.0 . Also connect the Data Communications Equipment to this connector.

3. Set the DCE/DTE switch to the "DCE" position.

4. Set the external transmit timing switch to the "off" position.

5. Set the data rate parameter to the baud rate of the asynchronous data.

6. Set the delay parameter to the desired delay.

7. Set the random error rate for each channel as described in the previous sections.

8. If burst errors are needed, set the burst length, gap length, and burst density as described in the previous sections.

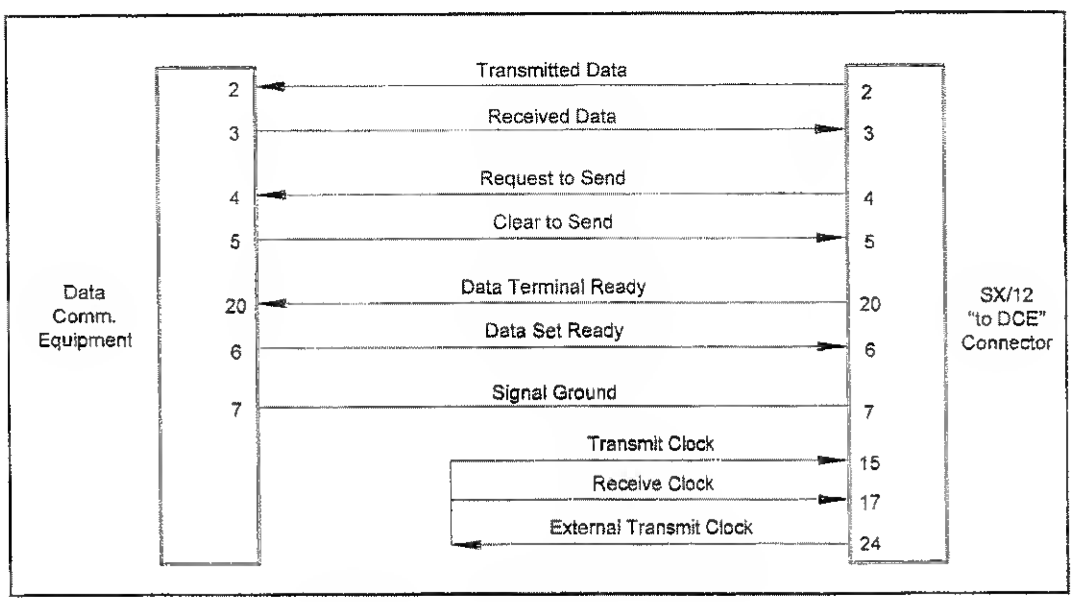

Figure 3.0 Asynchronous RS-232c Patch Cable

Chapter 4

Programming

Introduction

This chapter describes how to enter, edit and run a program on the SX/12. Programming allows the user to create complex error sequences for simulating the changing error conditions that can occur in real data channels. Alternatively, several "manually triggered" sequences of a few steps each can be entered to simulate different error scenarios. A repeating option may be programmed into the last step to repetitively expose the attached data communication devices to the channel disturbances defined by the program. Each program step may have different Gaussian and burst error characteristics. The delay and data rate can also be changed but should be done so when data discontinuity is not a concern. Using the optional IEEE-488 remote control interface, programs can be entered remotely or uploaded to and downloaded from the IEEE-488 controller. (See Appendix H.) The battery-backed memory of the SX/12 retains the program when power is lost.

The program may have up to 99 steps. Associated with each step are the delay, data rate, random error, burst error and step duration parameters. When the program runs, the steps are sequentially executed. Each step programs the SX/12 with its delay, data rate, random and burst error parameters. The step duration parameter in each step determines when the next step is executed. Step duration times range from 1 to 9,999,999 seconds. Special step duration options can be selected to make program execution wait for the [ENTER] key before continuing, or to repeat the program from the beginning. The normal SX/12 parameters are restored when the program execution is finished or stopped.

Operation

A program is entered and edited on the SX/12 by selecting the program edit mode with the [OPTIONS] key. The normal parameters will continue to function while in this mode. The SX/12 display will change to a display that alternates between the normal parameter display and a display that shows the edit mode, current step number and step duration. If the program memory is empty, the first step will be displayed with "END" displayed in place of the step duration to indicate the end of the program. The step parameters will be the same as the normal parameters. If the program memory is not empty, the current step from the last edit session will be displayed.

The following keys are used to enter and edit a program in the program edit mode.

[OPTIONS] - This key is used to enter and exit the program edit mode.

1. Press [OPTIONS] until the program edit prompt appears.
2. Press [ENTER] to enter the program edit mode.
3. Repeat steps 1 and 2 to exit the program edit mode.

[DATA RATE] - This key is used to enter the data rate parameter. The entry procedure is identical to that used in the normal mode. See Chapter 3.

[DELAY] - This key is used to enter the delay parameter. The entry procedure is identical to that used in the normal mode. See Chapter 3.

[EAST/WEST RANDOM ERROR RATE] - These two keys are used to enter the East and West random error rate parameters. The entry procedures are identical to that used in the normal mode. See Chapter 3.

[EAST/WEST BURST LENGTH] - These two keys are used to enter the East and West burst length parameters. The entry procedures are identical to that used in the normal mode. See Chapter 3.

[EAST/WEST GAP LENGTH] - These two keys are used to enter the East and West burst gap length parameters. The entry procedures are identical to that used in the normal mode. See Chapter 3.

[EAST/WEST BURST DENSITY] - These two keys are used to enter the East and West burst density parameters. The entry procedures are identical to that used in the normal mode. See Chapter 3.

[GOTO(4)] - When not used as a numeric key, it is an edit function key that allows you to jump to a desired step number without having to step over intervening steps. The SX/12 will stop at the End step or the Repeat step if the specified step number is greater.
1. Press [GOTO(4)].
2. Enter the desired step number, then press [ENTER].

[INS(5)] - When not used as a numeric key, it is an edit function key that inserts a new step into the program at the current step number. The step parameters that were previously at and above the current step are pushed up to make room for the new step. The parameters of the new current step will be the same as the parameters of the previous current step. The insert function is ignored if used at the End step.
1. Press [INS(5)].
2. The current step being displayed is the inserted step.

[COPY(6)] - When not used as a numeric key, it is an edit function key that copies the step parameters of the previous step into the current step. This function is useful when the parameters of the current step are similar to the step before it.
1. Press [COPY(6)].
2. The parameters of the current step will change to those of the previous step.

[DEL(7)] - When not used as a numeric key, it is an edit function key that deletes the current step from the program. The step parameters of the step above the current step are moved down to fill space left by the deleted step.
1. Press [DEL(7)].
2. The current step being displayed was previously above the current step.

[PCLR(8)] - When not used as a numeric key, it is an edit function that is used to clear the program memory.
1. Press [PCLR(8)].
2. A prompt will appear to notify the user that the program is about to be cleared.
3. Press [ENTER] to clear the memory.

[DUR(9)] - When not used as a numeric key, it is an edit function that sets the step duration time of the current step. Special options within the step duration function can also be selected with the [SELECT] key. The first option "Step duration(sec)?   then go to 1", causes program execution to repeat the program from step 1 after waiting the duration time that was entered. This options allows a program sequence to repeat indefinitely until stopped by the user. The second option "Manual step trigger?", causes the program execution to wait for the [ENTER] key before continuing on to the next step. This option is useful for separating different program sequences. The program sequences are then triggered when the other equipment in the test are ready. With the optional SX/12 IEEE-488 remote control interface installed, the IEEE-488 Group Trigger command can be used to trigger the next sequence along with any other equipment hooked up to the IEEE-488 bus.

Entering the step duration time:
1. Press [DUR(9)].
2 Press [SELECT] until the duration entry prompt appears.
3. Enter the step duration time in seconds. The [x 10^3] and [x 10^6] keys can be used to speed up large entries.
4. Press the [ENTER] key to complete the entry.
5. The step duration time is indicated on the lower left corner of the step display preceded with the prompt "t=".

Selecting the program repeat option:
1. Press [DUR(9)].
2 Enter the step duration time in seconds. The [x 10^3] and [x 10^6] keys can be used to speed up large entries.
3. Press the [SELECT] key until the repeat option is displayed.
4. Press the [ENTER] key to complete the entry.
5. The repeat option is indicated on the step display with a "R" appended to the step duration time.

Selecting the manual step trigger option:
1. Press [DUR(9)].
2. Press the [SELECT] key until the manual trigger prompt appears.
3. Press the [ENTER] key to complete the entry.
4. The manual step trigger option is indicated on the step display with the prompt "Man Trig" displayed in place of the step duration time.

[STOP(.)] - When not used as a decimal key, it is an edit function key that is used to stop the execution of the program. This key functions in both the normal and program editing mode.
1. Press [STOP(.)].
2. The display will display the step that the program stopped on in the program edit mode, or display the normal parameters in the normal mode.

[RUN(0)] - When not used as a numeric key, it is an edit function key that starts the execution of the program. If pressed in the normal mode, the program begins execution from step one. If pressed in the program edit mode, the program begins execution from the current step. The program execution is indicated by a faster alternating display with "RUN" displayed in place of "EDIT". The step that is displayed is the step that was just executed.
1. Press [RUN(0)].
2. If a program is present, "RUN" will be displayed on the left side of the display.

[SELECT] - When not used to select options, it is an edit function key that steps the program back a step each time it is pressed. This key is ignored if the current step number is 1.
1. Press [SELECT].
2. The previous step will be displayed and become the current step.

[ENTER] - When not used to enter parameters, it is an edit function key that steps the program forward a step each time it is pressed. This key is ignored if the current step has the program repeat option. When pressed at End step, the step duration function is entered to obtain a duration time from the user before moving to the next step.
1. Press [ENTER].
2. The next step will be displayed and become the current step.

Programming Examples

Example 1:
The data channel is a radio frequency telemetry link between a mother and a daughter ship. Special FEC (forward error corrector) hardware and ARQ (automatic request) software was developed to reliably transfer the data between the two ships under severe ocean conditions. The following channel conditions need to be simulated for the bench-test of the new hardware and software.

Data rate: 6.312 Mbits/s
Delay: 100 bytes due to the transmission equipment
Gaussian error rate: $1e^{-4}$ errors/bit
Short fade: errors increase to .5 errors/bit for an average length of 200 ms once every second
Long fade: errors increase to .5 errors/bit for an average length of 10 seconds once every minute

These channel conditions can be simulated with a two step program on the SX/12. The following describes the program entry:

First set the normal parameters. (These parameters are used as defaults for the new program steps).

1. Press [DATA RATE] and enter 6.312 and [x10^6] to set the data rate.
2. Press [DELAY], enter 100, then press [SELECT] until "bytes" is selected and press [ENTER] to set the delay.
3. Press [RANDOM ERROR RATE EAST], enter 0 and press [ENTER] to turn off the East Gaussian errors
4. Press [RANDOM ERROR RATE WEST], enter 0, and press [ENTER] to turn off the West Gaussian errors.
5. Press [BURST LENGTH EAST], enter 0, and press [ENTER].
6. Press [GAP LENGTH EAST], enter 0, and press [ENTER].
7. Press [BURST DENSITY EAST], enter 0, and press [ENTER] to turn off the East burst errors.
8. Press [BURST LENGTH WEST], enter 0, and press [ENTER].
9. Press [GAP LENGTH WEST], enter 0, and press [ENTER].
10. Press [BURST DENSITY WEST], enter 0, and press [ENTER] to turn off the West burst errors.

Next enter the program edit mode.

1. Press [OPTIONS] until the program edit prompt appears, then [ENTER] to enter the program edit mode.
2. Press [PCLR(8), then [ENTER] to erase the program memory and begin at program step 1.

Enter the $1e^{-4}$ Gaussian errors on program step 1.

1. Press [RANDOM ERROR RATE EAST], enter 1, [ENTER], 4, and [ENTER] to enter the East Gaussian error.
2. Press [RANDOM ERROR RATE WEST], enter 1, [ENTER], 4, and [ENTER] to enter the West Gaussian error.

Also, enter the short fade error on program step 1.

1. Press [BURST LENGTH EAST], enter 200, then press [SELECT] until "ms - random" is selected and press [ENTER] to set the East 200ms average burst length.
2. Press [BURST LENGTH WEST], enter 200, then press [SELECT] until "ms - random" is selected and press [ENTER] to set the West 200ms average burst length.

3. Press [GAP LENGTH EAST], enter .8 and [x10^3], then press [SELECT] until "fixed" is se- lected and press [ENTER] to set the East .8 second gap length.
7. Press [GAP LENGTH WEST], enter .8 and [x10^3], then press [SELECT] until "fixed" is selected and press [ENTER] to set the West .8 second gap length.
8. Press [BURST DENSITY EAST], enter 5, [ENTER], 1, and [ENTER] to enter the East burst density of .5 errors/bit.
9. Press [BURST DENSITY WEST], enter 5, [ENTER], 1, and [ENTER] to enter the West burst density of .5 errors/bit.
10. Press [DUR(9)], enter 50 and press [ENTER] to allow the Gaussian and short fade errors to run for 50 seconds.

Step to program step 2.

1. Press [ENTER] to move to the next step.

Enter the long fade error in program step 2.

1. Press [RANDOM ERROR RATE EAST], enter 5, [ENTER], 1, and [ENTER] to enter the .5 er- ror rate for the long fade on the East channel.
2. Press [RANDOM ERROR RATE WEST], enter 5, [ENTER], 1, and [ENTER] to enter the .5 er- ror rate for the long fade on the West channel.
3. Press [DUR(9)], enter 10, then press [SELECT] to choose the "go to 1" option and press [EN- TER]. This will cause the long fade errors to run for 10 seconds before repeating over from step 1

Leave the program edit mode.

1. Press [OPTIONS] until the program edit prompt appears, then [ENTER] to leave the pro- gram edit mode.

Running and stopping the program.

1. Press [RUN(0)]. The program that was just entered will begin from step 1 and run indefinitely until [STOP(.)] is pressed.

Example 2:

A terrestrial T1 data channel with a backup satellite channel needs to be simulated to test the resynchronizing ability of the T1 multiplexers when the channel is switched. The terrestrial and satellite channel conditions are as follows:

Terrestrial Channel:
Data Rate: 1.544 Mbits/s
Delay: 2ms
Gaussian error rate: 1e^{-7} errors/bit
Burst error characteristics: 10 bits average length, occurring at an average rate of 1 Hz.

Satellite Channel:
Data Rate: 1.544 Mbits/s
Delay: 240 ms
Gaussian error rate: 5e^{-8} errors/bit

The following program can be used to repeatedly "switch" between the terrestrial and satellite data channels every 10 minutes.

Step 1:
Data Rate = 1.544 MHz
Delay = 2 ms
East/West Random Error Rate = 1e^{-7}

East/West Burst Length = 10bR (10 bits average, randomize)
East/West Gap Length = 1000R (1 second average gap length, randomize)
East/West Burst Density = $5e^{-1}$
Step Duration = 600 (wait 10 minutes)

Step 2:
Data Rate = 1.544 MHz
Delay = 240 ms
East/West Random Error Rate = $5e^{-8}$
East/West Burst Length = 0bR
East/West Gap Length = 0 (manual, burst errors turned off)
East/West Burst Density = 0
Step Duration = 600R (wait 10 minutes and repeat program)

Example 3:
The testing department of a T1 multiplexer manufacturer needs to test their multiplexors under various error conditions as part of their test procedure. Using an SX/12 to simulate the T1 data channel, the following program will allow the user to simulate the various error conditions. By using the manual step trigger option between the different error sequences in the program, the user can trigger the start of the next error condition with the [ENTER] key.

Normal Parameters - T1 rate, satellite delay
Data Rate = 1.544 MHz
Delay = 240 ms
East/West Random Error Rate = 0
East/West Burst Length = 0bF
East/West Gap Length = Manual
East/West Burst Density = 0

Error Condition 1 - Gaussian errors at $1e^{-7}$ errors/bit
Step 1
Data Rate = 1.544 MHz
Delay = 240 ms
East/West Random Error Rate = $1e^{-7}$
East/West Burst Length = 0bF
East/West Gap Length = Manual
East/West Burst Density = 0
Step Duration = Manual Trigger

Error Condition 2 - Gaussian errors at $5e^{-5}$ errors/bit
Step 2
Data Rate = 1.544 MHz
Delay = 240 ms
East/West Random Error Rate = $5e^{-5}$
East/West Burst Length = 0bF
East/West Gap Length = Manual
East/West Burst Density = 0
Step Duration = Manual Trigger

Error Condition 3 - Gaussian errors at $2e^{-3}$ errors/bit
Step 3
Data Rate = 1.544 MHz

Delay = 240 ms
East/West Random Error Rate = $2e^{-3}$
East/West Burst Length = 0bF
East/West Gap Length = Manual
East/West Burst Density = 0
Step Duration = Manual Trigger

Error Condition 4 - 10ms average error bursts at $2e^{-5}$ errors/bit, 200ms average gaps with Gaussian errors at $2e^{-9}$ errors/bit.

Step 4
Data Rate = 1.544 MHz
Delay = 240 ms
East/West Random Error Rate = $2e^{-9}$
East/West Burst Length = 10msR
East/West Gap Length = 200R
East/West Burst Density = $2e^{-5}$
Step Duration = Manual Trigger

Error Condition 5 - Severe rainstorm simulation

Step 5 ($2e^{-9}$ Gaussian errors.)
Data Rate = 1.544 MHz
Delay = 240 ms
East/West Random Error Rate = $2e^{-9}$
East/West Burst Length = 0msR
East/West Gap Length = Manual
East/West Burst Density = 0
Step Duration = 100

Step 6 ($3e^{-8}$ Gaussian errors)
Data Rate = 1.544 MHz
Delay = 240 ms
East/West Random Error Rate = $3e^{-8}$
East/West Burst Length = 0msR
East/West Gap Length = Manual
East/West Burst Density = 0
Step Duration = 100

Step 7 ($4e^{-7}$ Gaussian errors)
Data Rate = 1.544 MHz
Delay = 240 ms
East/West Random Error Rate = $4e^{-7}$
East/West Burst Length = 0msR
East/West Gap Length = Manual
East/West Burst Density = 0
Step Duration = 100

Step 8 ($5e^{-6}$ Gaussian errors)
Data Rate = 1.544 MHz
Delay = 240 ms
East/West Random Error Rate = $5e^{-6}$
East/West Burst Length = 0msR
East/West Gap Length = Manual

East/West Burst Density = 0
Step Duration = 100

Step 9 ($6e^{-5}$ Gaussian errors with severe random burst errors, 50ms average length, 5 seconds average gap)
Data Rate = 1.544 MHz
Delay = 240 ms
East/West Random Error Rate = $6e^{-5}$
East/West Burst Length = 50msR
East/West Gap Length = 5000R
East/West Burst Density = $5e^{-1}$
Step Duration = 200

Step 10 ($7e^{-6}$ Gaussian errors)
Data Rate = 1.544 MHz
Delay = 240 ms
East/West Random Error Rate = $7e^{-6}$
East/West Burst Length = 0msR
East/West Gap Length = Manual
East/West Burst Density = 0
Step Duration = 100

Step 11 ($8e^{-7}$ Gaussian errors)
Data Rate = 1.544 MHz
Delay = 240 ms
East/West Random Error Rate = $8e^{-7}$
East/West Burst Length = 0msR
East/West Gap Length = Manual
East/West Burst Density = 0
Step Duration = 100

Step 12 ($9e^{-8}$ Gaussian errors)
Data Rate = 1.544 MHz
Delay = 240 ms
East/West Random Error Rate = $9e^{-8}$
East/West Burst Length = 0msR
East/West Gap Length = Manual
East/West Burst Density = 0
Step Duration = 100

Step 13 ($2e^{-9}$ Gaussian errors)
Data Rate = 1.544 MHz
Delay = 240 ms
East/West Random Error Rate = $2e^{-9}$
East/West Burst Length = 0msR
East/West Gap Length = Manual
East/West Burst Density = 0
Step Duration = Manual Trigger

Repeat error conditions
Step 14
Data Rate = 1.544 MHz

Delay = 240 ms
East/West Random Error Rate = 0
East/West Burst Length = 0msR
East/West Gap Length = Manual
East/West Burst Density = 0
Step Duration = 1R

Appendix A
SX/12 Specifications

Type of Channel:

Full-duplex

Random Bit Error Rates: (err/bit)

0,1x10^{-9}, 2x10^{-9},3x10^{-9}, ... 9x10^{-1}, 1

Burst Error Density: (err/bit)

0,1x10^{-9}, 2x10^{-9},3x10^{-9}, ... 9x10^{-1}, 1

Burst Length: (selectable)

1, 2, 3, ... 16,777,215 bits fixed length
1, 2, 3, ... 16,777,215 bits random length
1, 2, 3, ... 9,999 ms fixed length
1, 2, 3, ... 9,999 ms random length

Gap Length: (selectable)

1, 2, 3, ... 99,999,999 ms fixed length
1, 2, 3, ... 40,950,000 ms random length

Burst Modes:

Fixed gap length, fixed burst length
Random gap length, fixed burst length
Fixed gap length, random burst length
Random gap length, random burst length
Manual burst trigger, fixed burst length
Manual burst trigger, random burst length

Data Rates: (bits/sec)

SX/12-0 100, 200, 300, ... 100,000
SX/12-1 100, 200, 300, ... 2,048,000
SX/12-2 100, 200, 300, ... 8,448,000

Channel Delay: (selectable) Delay in each direction.

0, 1, 2, ... 9,999 ms
0, 1, 2, ... 9,999 bytes

Maximum Channel Delay at Maximum Data Rate: (msec.)

SX/12-0 655
SX/12-1 1000
SX/12-2 992

Program:

99 parameter steps.
Programmable parameters include step duration, delay, data rate, random errors and burst errors.
Special steps include: wait for manual trigger, repeat program.

SX/12 SPECIFICATIONS

Power: (±10%)

115 or 230 VAC, 48 to 66 Hz

Operating Temperature:

0 to 55 degrees C (31 to 131 degrees F), 20 to 30 degrees C recommended

Humidity:

10% to 90%, noncondensing

Dimensions:

19"(48.3 cm)W x 3.5"(8.89 cm)H x 12"(30.48 cm)D

Weight:

13 lb (5.85 kg)

Appendix B
SX/12 Error Functions

The SX/12 Data Channel Simulator performs a number of random effects. These include random error rate, burst densities, random burst lengths, and random gap lengths. The purpose of this section is to describe these effects.

Note that the effects described will pertain to both east and west channels and that the functioning of these effects on the two channels is independent of each other.

Error Indicators

Located along the right edge of the LCD display are a pair of red error indicators, one each for the East and West channels. These indicators flash to show the random and burst errors generated by each channel.

Random Error Rate

Random Error Rate (RER) is defined in units of errors per bit. These errors have the same distribution as errors caused by Gaussian noise. The RER is settable from 1×10^{-0} to 1×10^{-9} errors/bit. Setting the RER is generally done to achieve one of two effects:

1) The desired effect is an error occurring on the average, every n bits in the error stream. The solution is to set the RER to 1/n (or as near as it can be).

   Example: We want on the average 20,000 bits between errors.
   Set RER to $1/n = 1/20{,}000 = 5e^{-5}$.

2) It is desired to have errors occur at random intervals with a mean of T seconds between errors. The solution is to set the RER to 1/(fT) where f is the data rate in bits/sec and T is the desired time between errors in sec/error.

   Example: The data rate is 1.544×10^{6} bits/sec.
   We want errors to occur at approximately 3 millisecond intervals.
   Set RER to $1/(fT) = 2.159 \times 10^{-4} \approx 2e^{-4}$.

Note that random error operation is dependent upon burst error functioning. Namely, if RER is non-zero and burst error functions are operating at the same time, then a random error can occur only during the burst gap times, not during the burst error segment itself.

SX/12 ERROR FUNCTIONS

Burst Errors

The burst error features of the SX/12 offer the user more control over errors than the random error features do. Burst error functions allow the user to:

A) Achieve lower effective random error rates than by using the Random Error Rate parameter alone.

B) Generate consecutive bit errors to test effectiveness of error-correction schemes.

C) Generate errors at fixed time intervals to simulate periodic error sources.

D) Manually trigger errors, singly or in bursts.

The parameters for setting up burst error effects include burst length (bits or milliseconds), burst density (errors/bit), and gap length (msec). These effects are programmed separately for each channel and operate independently on each channel.

Burst Length

Burst length is measured in bits or in ms. A burst can be thought of as a "window" during which the burst error generator becomes active. The burst density parameter determines the error rate of the bits between the starting and ending bits of the this 'window.' Burst length can be a constant length (fixed) or can be made to vary (random). In random burst mode, the distribution of burst lengths is geometric with the mean being the entered burst length.

Burst Density

The burst density parameter defines the random error rate during the burst error "window." Functionally, burst error densities operate the same as Random Error Rates, except that they are active only during bursts. As with the random error rate, this error distribution is Gaussian, with the mean being the number entered.

Note that a burst always starts and ends with an error. The burst density parameter applies to the data stream only between these bits. Consequently, for burst lengths of 1 and 2, the burst density parameter does not apply. The effect of the starting and ending error bits is to add two additional errors to the errors determined by the burst density. This has the greatest impact when short error bursts are used. For example:

> If a burst length of 12 is specified and a burst density of $2e^{-1}$ is specified, then the expected number of errors for the burst is:
>
> $$2 \text{ (errs)} + [10 \text{ (bits)} \times 2e^{-1} \text{ (errs/bit)}] = 4 \text{ (errs)}$$
>
> So the effective burst density will be more like 4/12 errs/bit or approximately $3.3e^{-1}$ errs/bit.

The impact on the burst density due to the two additional errors quickly becomes negligible as longer error bursts are used.

Gap Length

The gap length parameter defines the time between bursts in milliseconds. Gap length can be constant (fixed) or made to vary (random). The distribution of random gap lengths is geometric with the mean being the number entered.

Burst Error Examples:

Ex. A: The data rate is 1.544 MHz and a random error rate of 1×10^{-10} in the east channel is desired. The burst error generator can be used to achieve lower error rates than can be achieved with the random error generator.

Solution: Set east random error rate to 0
Set east burst length to 1F
Set east burst density to $1e^{-0}$
Set east gap length to 6480000R

In general:

With burst length set to 1F, the gap length can be thought of as having dimensions of msec/error. To achieve effective random error rate Er:

Gr = 1000/(Er x f)

Where: Gr = gap length (msec)
Er = effective random error rate (errs/bit)
f = data rate (bit/sec)

Ex. B: An error-corrector is to pass flawless data even if four consecutive bits are errors and this needs to be tested.

Solution: Set burst length to 4F
Set burst density to $1e^{-0}$
Set gap length appropriately

Ex. C: A data channel is known to have a normal error rate of approximately 3×10^{-6} errors/bit. It is also known that every 5 minutes the error rate increases 100x for 8 seconds. The data rate is 1.544 MHz.

Solution: Set random error rate to $3e^{-6}$
Set gap length to 260000F { (5x(60-8))x1000 msec }
Set burst density to $3e^{-4}$
Set burst length to 8000msF

Ex. D: An engineer wants to inject triple bit error bursts into a data stream.

Solution: Set west gap length to 0F (MANUAL)
Set west burst density to $1e^{-0}$
Set west burst length to 3F (bits)
Set east gap length to 0F (MANUAL)
Set east burst density to $1e^{-0}$
Set east burst length to 3F (bits)
Press the [1] key when west channel burst desired
Press the [3] key when east channel burst desired
Press the [2] key for simultaneous errors in both channels

SX/12 ERROR FUNCTIONS

Appendix C
RS-232-C Interface

Description

The RS-232-C interface module is designed to convert between the TTL signals used within the SX/12 and signals complying with EIA standard RS-232-C. East and West female RS-232 "D" type connectors are provided for connecting to Data Terminal Equipments. A West male RS-232 "D" type connector is also provided for applications requiring hookup to Data Communications Equipment. Only a single West connector is used at a time and is selected by the DCE/DTE switch located on the rear panel of the SX/12.

Specifications

Maximum signalling rate - 20 kb/s

Data Polarity -	Function OFF; Signal Condition Mark; Binary "1"; Interchange voltage < -3 Volts Function ON; Signal Condition Space; Binary "0"; Interchange voltage > 3 Volts
Drivers -	Signal swing ; ±10 Volts into 7K ohms
Receivers -	Load Impedance; 3K to 7K ohms Maximum input voltage; ±25 Volts
Data timing -	Data received by the SX/12 is sampled on the ON to OFF transition of the timing signal. Data transmitted by the SX/12 is clocked on the OFF to ON transition of the timing signal.
Cabling -	Less than 50 feet recommended

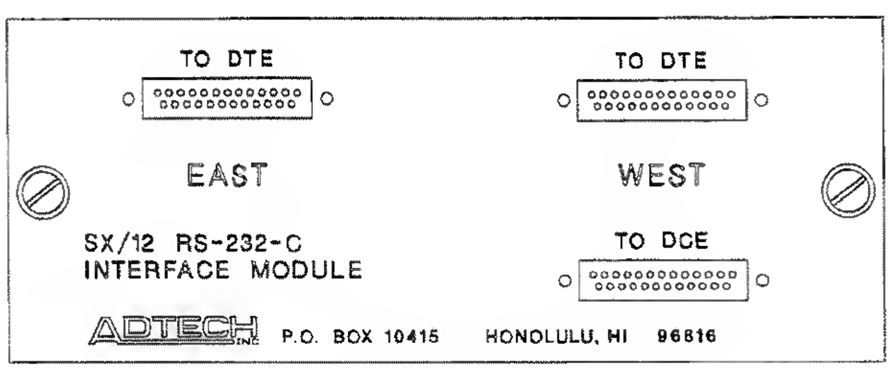

Figure C.1 RS-232-c Interface

Signalling Leads

DTE - DTE Configuration

East/West Connector:	CTS and RTS are connected together at each connector DSR and DCD are held "on"

DTE - DCE Configuration, delay > 0

East Connector:	CTS and RTS are connected together DSR and DCD are held "on"
West Connector:	RTS and DTR are held "on"

DTE - DCE Configuration, delay = 0

East/West Connector:	CTS (East) connected to CTS (West) RTS (East) connected to RTS (West) DSR (East) connected to DSR (West) DTR (East) connected to DTR (West)

Connector Pin Assignments

East "to DTE" Connector

Pin	Circuit	Signal	Lead Status
1	AA	Protective Ground	Strapped to interface panel
2	BA	Transmitted Data	West Channel Data Input
3	BB	Received Data	East Channel Data Output
4	CA	Request to Send	Input
5	CB	Clear to Send	Output
6	CC	Data Set Ready	Output
7	AB	Signal Ground	Internally connected to circuit ground
8	CF	Received Line Signal Detector	Output (Internally forced on)
15	DB	Transmit Signal Element Timing (DCE source)	Output
17	DD	Receive Signal Element Timing (DCE source)	Output
20	CD	Data Terminal Ready	Input
24	DA	Transmit Signal Element Timing (DTE source)	Input

West "to DTE" Connector

Pin	Circuit	Signal	Lead Status
1	AA	Protective Ground	Strapped to interface panel
2	BA	Transmitted Data	East Channel Data Input
3	BB	Received Data	West Channel Data Output
4	CA	Request to Send	Input (Internally strapped to CTS)
5	CB	Clear to Send	Output (Internally strapped to RST)
6	CC	Data Set Ready	Output (Internally forced on)
7	AB	Signal Ground	Internally connected to circuit ground
8	CF	Received Line Signal Detector	Output (Internally forced on)
15	DB	Transmit Signal Element Timing (DCE source)	Output
17	DD	Receive Signal Element Timing (DCE source)	Output
20	CD	Data Terminal Ready	Input
24	DA	Transmit Signal Element Timing (DTE source)	Input

West "to DCE" Connector

Pin	Circuit	Signal	Lead Status
1	AA	Protective Ground	Strapped to interface panel
2	BA	Transmitted Data	West Channel Data Output
3	BB	Received Data	East Channel Data Input
4	CA	Request to Send	Output
5	CB	Clear to Send	Input
6	CC	Data Set Ready	Input
7	AB	Signal Ground	Internally connected to circuit ground
8	CF	Received Line Signal Detector	Input (not connected)
15	DB	Transmit Signal Element Timing (DCE source)	Input
17	DD	Receive Signal Element Timing (DCE source)	Input
20	CD	Data Terminal Ready	Output
24	DA	Transmit Signel Element Timing (DTE source)	Output

RS-232-C INTERFACE

Appendix D

V.35 Interface

Description

The V.35 interface module is designed to convert between the TTL signals used within the SX/12 and signals complying with the CCITT recommendation V.35. East and West 34-pin connectors (Winchester MRA-34-P-JTC6-H8) are provided for connecting to Data Terminal Equipments. A West connector is also provided for applications requiring hookup to Data Communications Equipment. Only a single West connector is used at a time and is selected by the DCE/DTE switch located on the rear panel of the SX/12.

The V.35 interface uses high speed balanced V.35 type clock and data drivers and receivers. All signalling drivers and receivers are single-ended RS-232-C type.

Specifications

Maximum signalling rate - 10 Mb/s

Data Polarity -	Function OFF; Signal Condition Mark; Binary "1"; Data/Clock: Line A is nominally -.55 volts with respect to line B; Signalling leads: Interchange voltage < -3V Function ON; Signal Condition Space; Binary "0"; Data/Clock: Line A is nominally +.55 volts with respect to line B; Signalling leads: Interchange voltage > 3V
Drivers-	Data/Clock signal swing ; ±1.10 volts peak-to-peak into 100 ohms
Receivers -	Load Impedance for Data/Clock: 100 ohms; Signalling leads: 3k - 7k ohms
Data timing -	Data received by the SX/12 is sampled on the ON to OFF transition of the timing signal. Data transmitted by the SX/12 is clocked on the OFF to ON transition of the timing signal.
Cabling -	Less than 100 feet recommended

Jumper Options

Because data and clock signals do not travel exactly the same paths in the SX/12 and the outside world, the phase relationship between the data and clock signals can change as they travel along their circuits. At high speeds this phase change can be significant. Located on the interface module circuit board is a pair of jumper option blocks that allow the user to reclock the data. Selecting "yes" to this option reduces the output clock

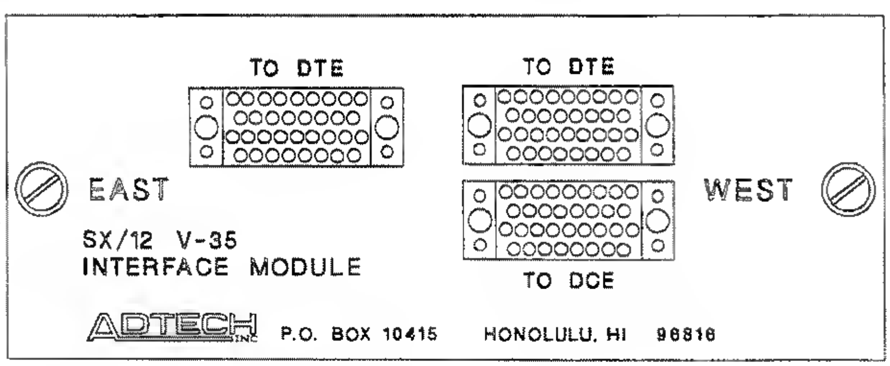

Figure D.1 V.35 Interface

to output data skew from 60 ns to approximately 10 ns. For the "to DTE" connectors, this affects the receive clock (SCR) to receive data (RD) skew. For the West "to DCE" connector, if the external transmit timing switch is "off", then the transmit clock (SCT) to transmit data (TD) skew is affected. If the external transmit timing switch is "on", then the external transmit clock (SCTE) to transmit data (TD) skew is affected. Selecting "yes" to this option adds a one bit delay which may not be desirable at low data rates.

Facing the back of the interface module, the reclocking options are located below the 50 pin flat cable connector. The Reclock East Data Out option is selected with the upper right jumper block. The Reclock West Data Out option is selected with the lower right jumper block.

Signalling Leads

DTE - DTE Configuration

East/West Connector:	CTS and RTS are connected together at each connector DSR and DCD are held "on"

DTE - DCE Configuration, delay > 0

East Connector:	CTS and RTS are connected together DSR and DCE are held "on"
West Connector:	RTS is held "on"

DTE - DCE Configuration, delay = 0

East/West Connector:	CTS (East) connected to CTS (West) RTS (East) connected to RTS (West) DSR (East) connected to DSR (West)

Connector Pin Assignments

East "to DTE" Connector

Pin	Circuit	Signal	Lead Status
A	AA	Protective Ground	Strapped to interface panel
B	AB	Signal Ground	Internally connected to circuit ground
C	CA	Request to Send	Input
D	CB	Clear to Send	Output
E	CC	Data Set Ready	Output
F	CF	Received Line Signal Detector	Output (Internally forced on)
P,S	SD(A,B)	Send Data	West channel data input
R,T	RD(A,B)	Received Data	East channel data output
U,W	SCTE(A,B)	Serial Clock Transmit External	Input
V,X	SCR(A,B)	Serial Clock Receive	Output
Y,a	SCT(A,B)	Serial Clock Transmit	Output

West "to DTE" Connector

Pin	Circuit	Signal	Lead Status
A	AA	Protective Ground	Strapped to interface panel
B	AB	Signal Ground	Internally connected to circuit ground
C	CA	Request to Send	Input (Internally looped to CTS)
D	CB	Clear to Send	Output (Internally looped to RTS)
E	CC	Data Set Ready	Output (Internally forced on)
F	CF	Received Line Signal Detector	Output (Internally forced on)
P,S	SD(A,B)	Send Data	East channel data input
R,T	RD(A,B)	Received Data	West channel data output
U,W	SCTE(A,B)	Serial Clock Transmit External	Input
V,X	SCR(A,B)	Serial Clock Receive	Output
Y,a	SCT(A,B)	Serial Clock Transmit	Output

West "to DCE" Connector

Pin	Circuit	Signal	Lead Status
A	AA	Protective Ground	Strapped to interface panel
B	AB	Signal Ground	Internally connected to circuit ground
C	CA	Request to Send	Output
D	CB	Clear to Send	Input
E	CC	Data Set Ready	Input
F	CF	Received Line Signal Detector	Input (Not used)
P,S	SD(A,B)	Send Data	West channel data output
R,T	RD(A,B)	Received Data	East channel data input
U,W	SCTE(A,B)	Serial Clock Transmit External	Output
V,X	SCR(A,B)	Serial Clock Receive	Input
Y,a	SCT(A,B)	Serial Clock Transmit	Input

V.35 INTERFACE

RS-422-A (RS-449) Interface

Description

The RS-422-A interface module is designed to convert between the TTL signals used within the SX/12 and signals complying with the EIA Standard RS-422-A. East and West female "D" type connectors are provided for connecting to Data Terminal Equipments. A male "D" type connector is also provided for applications requiring hookup to Data Communications Equipment. Only a single West connector is used at a time and is selected by the DCE/DTE switch located on the rear panel of the SX/12.

Specifications

Maximum signalling rate - 10 Mb/s

Data Polarity -	Function OFF; Signal Condition Mark; Binary "1"; Line A is more negative than line B Function ON; Signal Condition Space; Binary "0"; Line A is more positive than line B.
Drivers-	Signal swing; Balanced differential ±5 volts peak-to-peak into 100 ohms
Receivers -	Load Impedance; 220 ohms
Data timing -	Data received by the SX/12 is sampled on the ON to OFF transition of the timing signal. Data transmitted by the SX/12 is clocked on the OFF to ON transition of the timing signal.
Cabling -	Less than 200 feet recommended

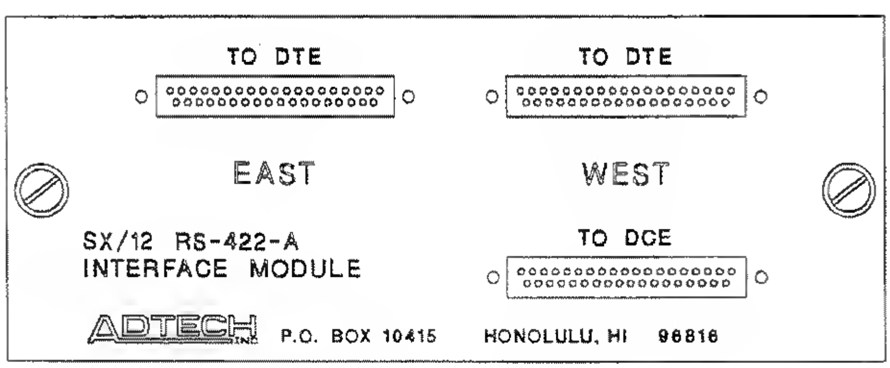

Figure E.1 RS-422-A Interface

Jumper Options

Because data and clock signals do not travel exactly the same paths in the SX/12 and the outside world, the phase relationship between the data and clock signals can change as they travel along their circuits. At high speeds this phase change can be significant. Located on the interface module circuit board is a pair of jumper option blocks that allow the user to reclock the data. Selecting "yes" to this option reduces the output clock to output data skew from 60 ns to approximately 10 ns. For the "to DTE" connectors, this affects the receive clock (RT) to receive data (RD) skew. For the West "to DCE" connector, if the external transmit timing switch is "off", then the transmit clock (ST) to transmit data (TD) skew is affected. If the external transmit timing switch is "on", then the external transmit clock (TT) to transmit data (TD) skew is affected. Selecting "yes" to this option adds a one bit delay which may not be desirable at low data rates.

Facing the back of the interface module, the reclocking options are located below and to the right of the 50 pin flat cable connector. The Reclock East Data Out option is selected with the right jumper block. The Reclock West Data Out option is selected with the left jumper block.

Signalling Leads

DTE - DTE Configuration

East/West Connector:	CTS and RTS are connected together at each connector DM and RR are held "on"

DTE - DCE Configuration, delay > 0

East Connector:	CTS and RTS are connected together DM and RR are held "on"
West Connector:	RTS and TR are held "on"

DTE - DCE Configuration, delay = 0

East/West Connector:	CTS (East) connected to CTS (West) RTS (East) connected to RTS (West) DM (East) connected to DM (West) TR (East) connected to TR (West)

Connector Pin Assignments

East "to DTE" Connector

Pin	Circuit	Signal	Lead Status
1	SHIELD	Protective Ground	Strapped to interface panel
2	SI	Signaling Rate Indicator	Output (Internally forced on)
4,22	SD(A,B)	Send Data	West channel data input
5,23	ST(A,B)	Send Timing	Output
6,24	RD(A,B)	Receive Data	East channel data output
7,25	RS(A,B)	Request to Send	Input
8,26	RT(A,B)	Receive Timing	Output
9,27	CS(A,B)	Clear to Send	Output
11,29	DM(A,B)	Data Mode	Output
12,30	TR(A,B)	Terminal Ready	Input
13,31	RR(A,B)	Receiver Ready	Output
15	IC	Incoming Call	Output (Internally forced off)
17,35	TT(A,B)	Terminal Timing	Input
18	Tm	Test Mode	Output (Internally forced off)
19	SG	Signal Ground	Internally connected to circuit ground
20	RC	Receive Common	Internally connected to circuit ground
33	SQ	Signal Quality	Output (Internally forced on)
36	Standby Indicator		Output (Internally forced off)
37	SC	Send Common	Internally connected to circuit ground

Connector Pin Assignment

West "to DTE" Connector

Pin	Circuit	Signal	Lead Status
1	SHIELD	Protective Ground	Strapped to interface panel
2	SI	Signaling Rate Indicator	Output (Internally forced on)
4,22	SD(A,B)	Send Data	East channel data input
5,23	ST(A,B)	Send Timing	Output
6,24	RD(A,B)	Receive Data	West channel data output
7,25	RS(A,B)	Request to Send	Input (Internally looped to CS)
8,26	RT(A,B)	Receive Timing	Output
9,27	CS(A,B)	Clear to Send	Output (Internally looped to RS)
11,29	DM(A,B)	Data Mode	Output (Internally forced on)
12,30	TR(A,B)	Terminal Ready	Input
13,31	RR(A,B)	Receiver Ready	Output (Internally forced on)
15	IC	Incoming Call	Output (Internally forced off)
17,35	TT(A,B)	Terminal Timing	Input
18	Tm	Test Mode	Output (Internally forced off)
19	SG	Signal Ground	Internally connected to circuit ground
20	RC	Receive Common	Internally connected to circuit ground
33	SQ	Signal Quality	Output (Internally forced on)
36	Standby Indicator		Output (Internally forced off)
37	SC	Send Common	Internally connected to circuit ground

Connector Pin Assignments

West "to DCE" Connector

Pin	Circuit	Signal	Lead Status
1	SHIELD	Protective Ground	Strapped to interface panel
2	SI	Signaling Rate Indicator	Open
4,22	SD(A,B)	Send Data	West channel data output
5,23	ST(A,B)	Send Timing	Input
6,24	RD(A,B)	Receive Data	East channel data input
7,25	RS(A,B)	Request to Send	Output
8,26	RT(A,B)	Receive Timing	Input
9,27	CS(A,B)	Clear to Send	Input
10	LL	Local Loopback	Output (Internally forced off)
11,29	DM(A,B)	Data Mode	Input
12,30	TR(A,B)	Terminal Ready	Output
13,31	RR(A,B)	Receiver Ready	Open
15	IC	Incoming Call	Open
16	SF/SR	Select Frequency/ Signalling Rate Indicator	Output (Internally forced on)
17,35	TT(A,B)	Terminal Timing	Output
18	Tm	Test Mode	Open
19	SG	Signal Ground	Internally connected to circuit ground
20	RC	Receive Common	Internally connected to circuit ground
28	IS	Terminal in Service	Output (Internally forced on)
32	SS	Select Standby	Output (Internally forced off)
33	SQ	Signal Quality	Open
34	Ns	New Signal	Output (Internally forced off)
36	Standby Indicator		Open
37	SC	Send Common	Internally connected to circuit ground

RS-422-A INTERFACE

Appendix F

DS1 (T1) Multi-clock and Standard Interfaces

Introduction

Two types of DS1 (T1) interfaces are currently available for the SX/12, the T1 Multi-clock Interface and the T1 Standard Interface. Both are described in this appendix. Read the appropriate description for your SX/12 T1 interface.

T1 Multiclock Interface

The T1 Multi-clock Interface Module is designed to convert between the TTL signals used within the SX/12 and signals complying with CCITT specification for 1.544 MHz T1 (DS-1) signals. East and West dual bantam jacks and 15 pin D type connectors are provided for receive and transmit data. LED indicators provide line status information. A BNC type connector provides a TTL level 1.544 MHz clock source, while a second BNC connector allows an external TTL level clock source to be used as a network clock. A transmit timing selector switch allows the SX/12 to be used in one of three different network timing configurations.

The T1 Multi-clock Interface Module has the following capabilities:

- East and West channels independently selectable for AMI and B8ZS coding.
- Transmitters modify transmit pulses internally for appropriate pulse shapes for lines up to 655 feet. Maximum range is greater than 1500 feet.
- Receiver sensitivity is -12dB.
- Receiver jitter tolerance is 300 UIs at 6 Hz to 0.4 UIs at 100 kHz.
- Interface is transparent to T1 framing.
- Interfaces with network equipment such as DACS, Channel Banks and DSX-1 cross connects.
- Interfaces with Customer Premises Equipment
- Three transmit timing modes for timing the T1 transmissions.
- Elastic buffer, size: 256 bits.

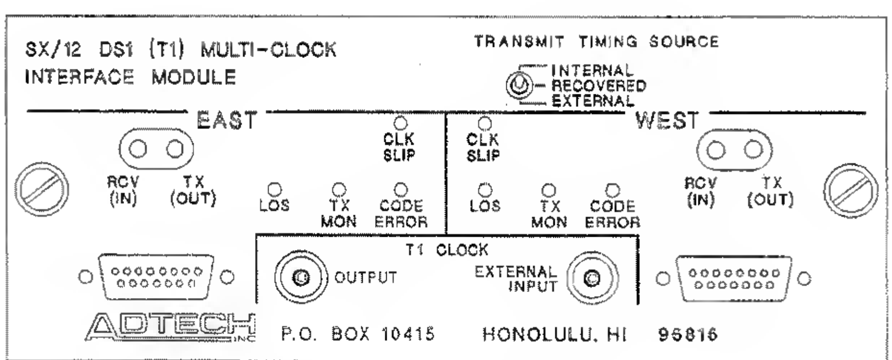

Figure F.1 Multiclock T1 Interface

Timing Configurations

Three transmit timing modes are selectable with the "TRANSMIT TIMING SOURCE" switch. These are Recovered Timing, Internal Timing and External Timing. The "CLK SLIP" indicator lights if a timing problem is detected, suggesting that an improper timing mode has been selected.

The Recovered Timing mode uses the clock recovered from the received data to time the data transmitted out of the SX/12. In this mode, the master clock is located in the external T1 equipment transmitting to the SX/12. Figure F.2 is a block diagram of this mode.

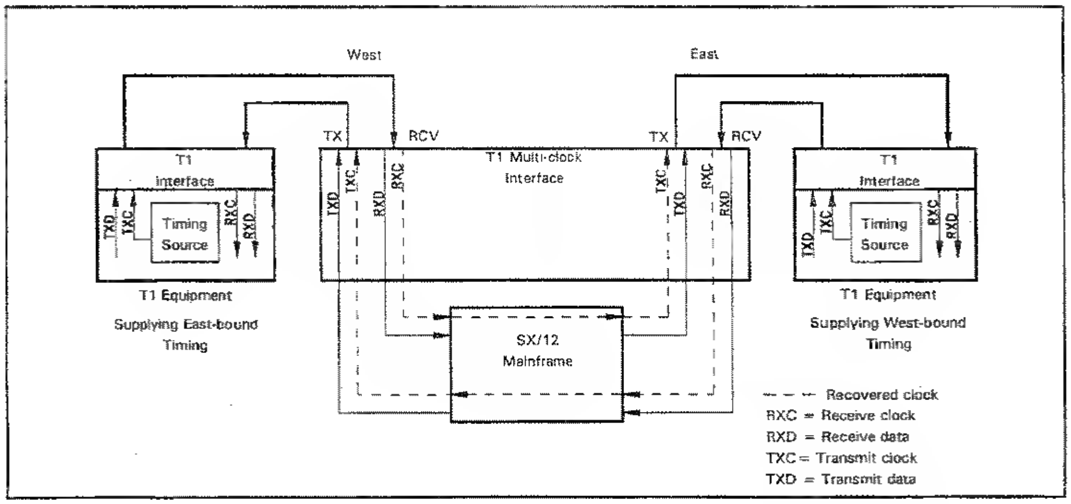

Figure F.2 Recovered Timing Mode

The Internal and External Timing modes allow the SX/12 to become the source of the master clock. The Internal Timing mode uses a highly accurate 1.544 MHz crystal oscillator located on the interface module as the master clock for East and West bound data. Figure F.3 is a block diagram of the Internal Timing mode.

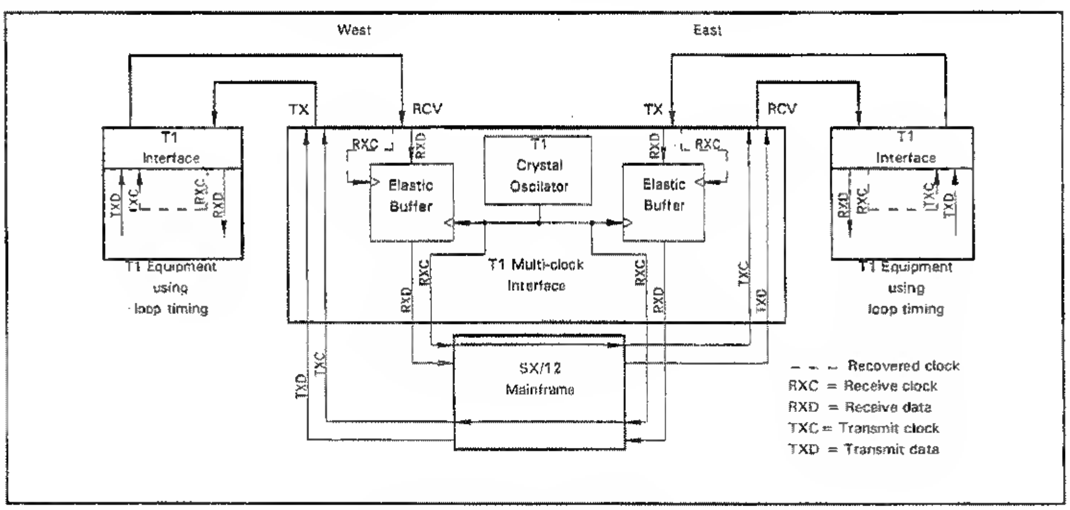

Figure F.3 Internal Timing Mode

The External Timing mode uses an external 1.544 MHz TTL (50 ohms) clock signal provided by the user as the master clock. This mode allows wander, jitter, and clock frequency errors to be injected by the external clock generator. It also allows multiple SX/12s to run off a single master clock. Figure F.4 is a block diagram of this mode.

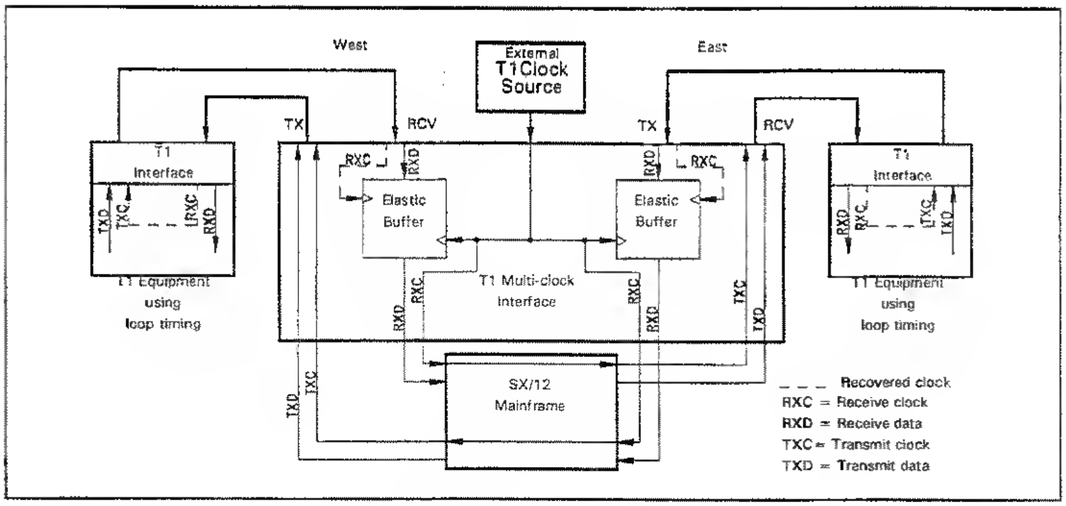

Figure F.4 External Timing Mode

You can choose one of these three modes with the three-position switch labeled "TRANSMIT TIMING SOURCE" on the interface module.

Operation

IMPORTANT: The T1 interface will only operate when the SX/12 External Transmit Timing Switch is in the "on" position.

The data rate on the SX/12 should be set to 1.544 MHz. Select the proper line coding and line pre-equalization with the dip switches located on the underside of the T1 Multiclock Interface module. The dip switches are described next.

Dip Switch 1

This dip switch sets the East and West line codes. Various line testing options are also available for the East and West channels.

Switch Position	Description
1	ETAO - East Transmit All Ones
2	ELL - East Local Loopback
3	ERL - East Remote Loopback
4	EC0 - East Code Select 0
5	EC1 - East Code Select 1
6	WTAO - West Transmit All Ones
7	WLL - West Local Loopback
8	WRL - West Remote Loopback
9	WC0 - West Code Select 0
10	WC1 - West Code Select 1

ETAO, WTAO - Setting to "1" causes continuous ones to be transmitted.
ELL, WLL - Setting to "1" routes the transmit clock and data from the SX/12 back into the SX/12 via the receive clock and data inputs of that port.
ERL, WRL - Setting to a "1" routes the recovered clock and receive data through the T1 driver of that port and back onto the line.
EC0, EC1, WC0, WC1 - Allow setting of code type for a particular channel as follows:

C0	C1	Code
0	0	AMI
0	1	B8ZS

Dip Switch 2

Line length selection offers pre-equalization of the output pulse for ABAM and PIC cables. Line length can be up to 655 feet. For each line length selected, the T1 interface transmitter modifies the output pulse to meet the requirements of ATT Compatibility Bulletin 119. When using cable other than ABAM or equivalent, it is recommended that optimal line length settings be determined by experiment.

Switch Position	Description
1	EL0 - East Length Select 0
2	EL1 - East Length Select 1
3	EL2 - East Length Select 2
4	WL0 - West Length Select 0
5	WL1 - West Length Select 1
6	WL2 - West Length Select 2

Switch Settings			Line Length
WL0 EL0	WL1 EL1	WL2 EL2	
1	1	0	0 - 133 feet
0	0	1	133 - 266 feet
1	0	1	266 - 399 feet
0	1	1	399 - 533 feet
1	1	1	533 - 655 feet
0	1	0	Part 68, Option A (CSU)
1	1	0	TICI.2 (CSU)

Specifications

Transmitter:

Output pulse amplitude: 2.4V - 3.6V (3.0V nominal).
Pre-equalizes for line lengths up to 655 feet.
Complies with ATT CB 119.

Receiver:

Sensitivity: -12dB (1.5 Vpp).
Allowable Consecutive Zeros before LOS: 160 - 190 (175 nominal)
Jitter tolerance: Better than 300 UIs at 6 Hz, 0.4 UIs 10 kHz to 100kHz.
Input impedance: 100 ohms.
Transparent to framing.

Clock Generator Output:

TTL level into 50 ohms.
BNC female connector
1.544 MHz ±25 ppm

External Clock Input:

Input voltage: TTL levels

Input impedance: 50 ohms.

Input frequency: 1.544 MHz (jitter and frequency error can also be added)

TX, RX Connector:

Dual bantam connector

Network connector:

15 pin female D connector

Pin	Signal
1	Send to network tip
9	Send to network ring
2	Chassis ground
3	Receive from network tip
11	Receive from network ring
4	Chassis ground

Interface Panel Indicators:

LOS - Loss Of Signal is lit when 175 consecutive zeros have been received. Indicator goes off when the received signal returns to 12.5% ones density, based on 4 ones out of 32 bit periods.

TX MON - Transmitter Monitor is lit if no signal is present on the transmitter tip and ring for 63 consecutive clock cycles.

CODE ERROR - Code Error is lit if a violation of the line coding scheme is detected.

CLK SLIP - Clock Slip is lit when the Elastic Buffer overflows or underflows. This will occur when the clocked data on the RCV line is not at the same nominal frequency as the internal or external source clock.

T1 Standard Interface

The T1 Standard Interface Module is designed to convert between the TTL signals used within the SX/12 and signals complying with CCITT specification for 1.544 MHz T1 (DS-1) signals. East and West dual bantam jacks and 15 pin D type connectors are provided for receive and transmit data. LED indicators provide line status information. A BNC type connector provides a TTL level clock source. Timing for the East and West-bound T1 data streams are generated by the external T1 equipment.

The T1 Standard Interface Module has the following capabilities:

- East and West channels independently selectable for AMI and B8ZS coding.
- Transmitters modify transmit pulses internally for appropriate pulse shapes for lines up to 655 feet. Maximum range is greater than 1500 feet.
- Receiver sensitivity is -12dB.
- Receiver jitter tolerance is 300 UIs at 6 Hz to 0.4 UIs at 100 kHz.
- Interface is transparent to T1 framing.
- Interfaces with network equipment such as DACS, Channel Banks and DSX-1 cross connects.
- Interfaces with Customer Premises Equipment

Operation

IMPORTANT: The T1 interface will only operate when the SX/12 External Transmit Timing Switch is in the "on" position.

The data rate on the SX/12 should be set to 1.544 MHz. Select the proper line coding and line pre-equalization with the dip switches on the T1 interface module. The dip switches are described next.

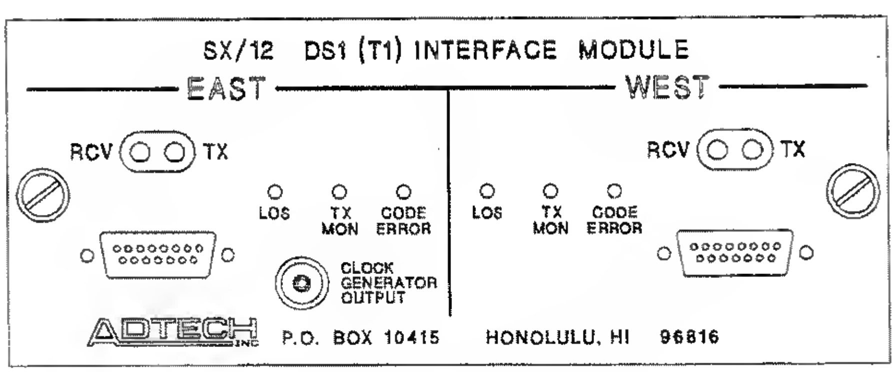

Figure F.5 Standard T1 Interface

Dip Switch 1

This dip switch sets the East and West line codes. Various line testing options are also available for the East and West channels.

Switch Position	Description
1	ETAO - East Transmit All Ones
2	ELL - East Local Loopback
3	ERL - East Remote Loopback
4	EC0 - East Code Select 0
5	EC1 - East Code Select 1
6	WTAO - West Transmit All Ones
7	WLL - West Local Loopback
8	WRL - West Remote Loopback
9	WC0 - West Code Select 0
10	WC1 - West Code Select 1

ETAO, WTAO - Setting to "1" causes continuous ones to be transmitted.
ELL, WLL - Setting to "1" routes the transmit clock and data from the SX/12 back into the SX/12 via the receive clock and data inputs of that port.
ERL, WRL - Setting to a "1" routes the recovered clock and receive data through the T1 driver of that port and back onto the line.
EC0, EC1, WC0, WC1 - Allow setting of code type for a particular channel as follows:

C0	C1	Code
0	0	AMI
0	1	B8ZS

Dip Switch 2

Line length selection offers pre-equalization of the output pulse for ABAM and PIC cables. Line length can be up to 655 feet. For each line length selected, the T1 interface transmitter modifies the output pulse to meet the requirements of ATT Compatibility Bulletin 119. When using cable other than ABAM or equivalent, it is recommended that optimal line length settings be determined by experiment.

Switch Position	Description
1	EL0 - East Length Select 0
2	EL1 - East Length Select 1
3	EL2 - East Length Select 2
4	WL0 - West Length Select 0
5	WL1 - West Length Select 1
6	WL2 - West Length Select 2

Switch Settings

WL0 EL0	WL1 EL1	WL2 EL2	Line Length
1	1	0	0 - 133 feet
0	0	1	133 - 266 feet
1	0	1	266 - 399 feet
0	1	1	399 - 533 feet
1	1	1	533 - 655 feet
0	1	0	Part 68, Option A (CSU)
1	1	0	TICI.2 (CSU)

DS1 (T1) MULTI-CLOCK AND STANDARD INTERFACES

Specifications

Transmitter:

Output pulse amplitude: 2.4V - 3.6V (3.0V nominal).
Pre-equalizes for line lengths up to 655 feet.
Complies with ATT CB 119.

Receiver:

Sensitivity: -12dB (1.5 Vpp).
Allowable Consecutive Zeros before LOS: 160 - 190 (175 nominal)
Jitter tolerance: Better than 300 UIs at 6 Hz, 0.4 UIs 10 kHz to 100kHz.
Input impedance: 100 ohms.
Transparent to framing.

Clock Generator Output:

TTL level into 50 ohms.
BNC female connector

TX, RX Connector:

Dual bantam connector

Network connector:

15 pin female D connector

Pin	Signal
1	Send to network tip
9	Send to network ring
2	Chassis ground
3	Receive from network tip
11	Receive from network ring
4	Chassis ground

Interface Panel Indicators:

LOS - Loss Of Signal is lit when 175 consecutive zeros have been received. Indicator goes off when the received signal returns to 12.5% ones density, based on 4 ones out of 32 bit periods.

TX MON - Transmitter Monitor is lit if no signal is present on the transmitter tip and ring for 63 consecutive clock cycles.

CODE ERROR - Code Error is lit if a violation of the line coding scheme is detected.

G.703 (2048kbps) Multi-clock and Standard Interfaces

Introduction

Two types of G.703 (2048 KBPS) interfaces are currently available for the SX/12, the G.703 Multi-clock Interface and the G.703 Standard Interface. Both are described in this appendix. Read the appropriate description for your SX/12 G.703 interface.

G.703 Multi-clock Interface

The G.703 Multi-clock Interface Module is designed to convert between the TTL signals used within the SX/12 and signals complying with CCITT G.703 specification for 2.048 MHz signals. East and West dual bantam jacks and 15 pin D type connectors are provided for receive and transmit data. Adapters for BNC and Twinax connectors are also available. LED indicators provide line status information. A BNC type connector provides a TTL level 2.048 MHz clock source, while a second BNC connector allows an external TTL level clock source to be used as a network clock. A transmit timing selector switch allows the SX/12 to be used in one of three different network timing configurations..

The G.703 Multi-clock Interface Module has the following capabilities:

- East and West channels can independently select AMI, B8ZS, B6ZS, and HDB3 coding.
- Maximum range is greater than 1500 feet.
- Receiver sensitivity is -12dB.
- Receiver jitter tolerance is 300 UIs at 6 Hz to 0.4 UIs at 100 kHz.
- Interface is transparent to signal data framing.
- East and West channels can independently select 75 or 120 ohm receiver impedance for coaxial or twisted pair cables.
- Interface is transparent to G.703 framing.
- Interfaces with network equipment such as DACS, Channel Banks and DSX-1 cross connects.

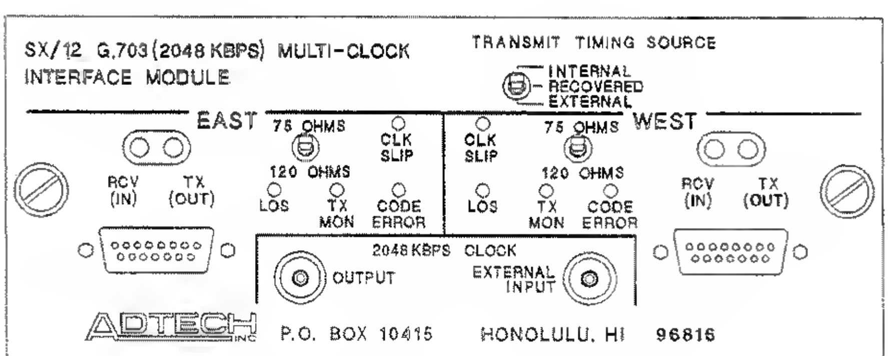

Figure G.1 G.703 (2.048 MHz) Multi-clock Interface

- Interfaces with Customer Premises Equipment
- Three transmit timing modes for timing the G.703 transmissions.
- Elastic buffer, size: 256 bits.

Timing Configurations

Three transmit timing modes are selectable with the "TRANSMIT TIMING SOURCE" switch. These are Recovered Timing, Internal Timing and External Timing. The "CLK SLIP" indicator lights if a timing problem is detected, suggesting that an improper timing mode has been selected.

The Recovered Timing mode uses the clock recovered from the received data to time the data transmitted out of the SX/12. In this mode, the master clock is located in the external G.703 equipment transmitting to the SX/12. Figure G.2 is a block diagram of this mode.

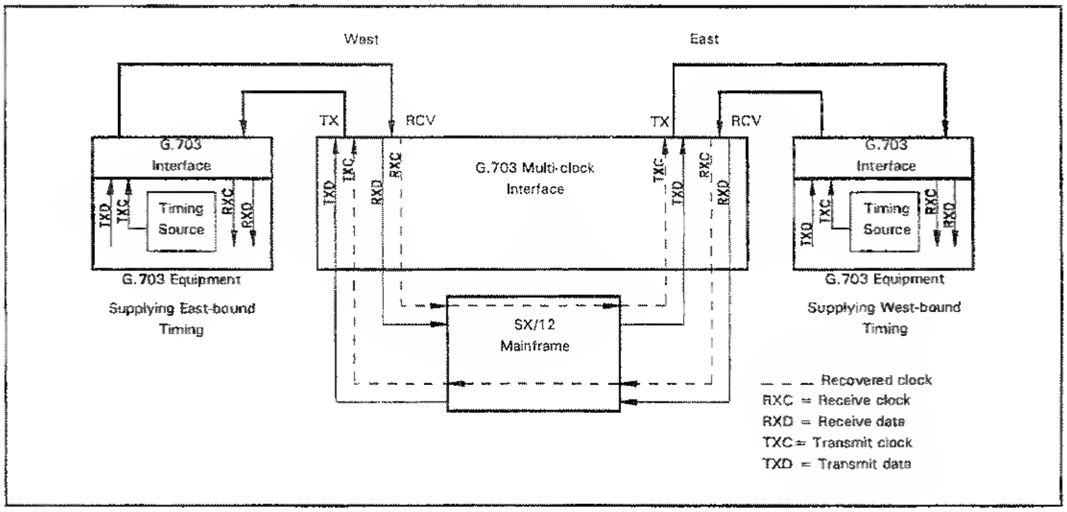

Figure G.2 Recovered Timing Mode

The Internal and External Timing modes allow the SX/12 to become the source of the master clock. The Internal Timing mode uses a highly accurate 2.048 MHz crystal oscillator located on the interface module as the master clock for East and West bound data. Figure G.3 is a block diagram of the Internal Timing mode.

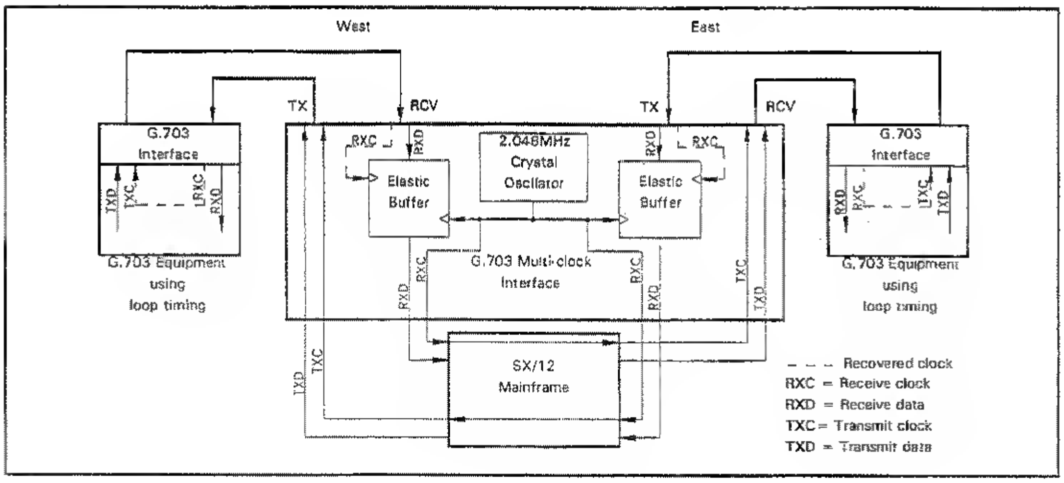

Figure G.3 Internal Timing Mode

The External Timing mode uses an external 2.048 MHz TTL (50 ohms) clock signal provided by the user as the master clock. This mode allows wander, jitter, and clock frequency errors to be injected by the external clock generator. It also allows multiple SX/12s to run off a single master clock. Figure G.4 is a block diagram of this mode.

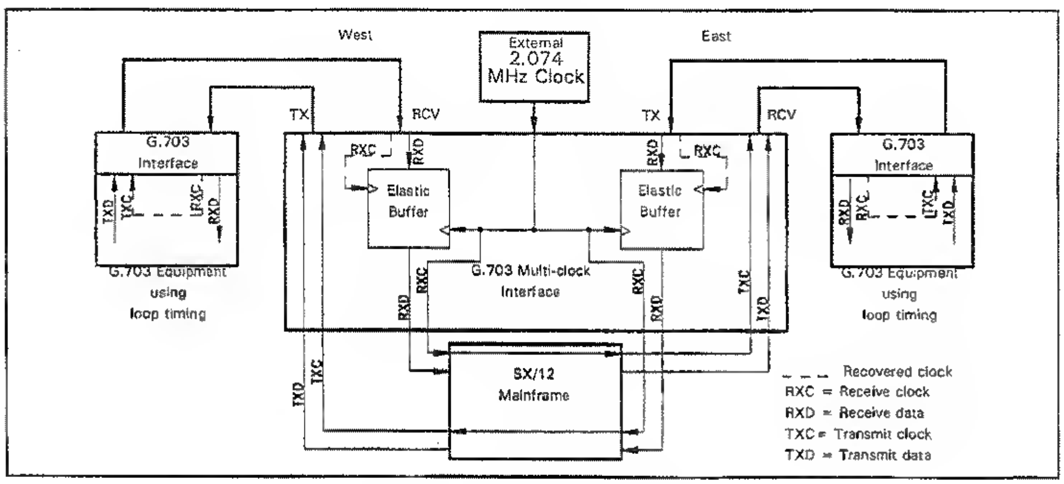

Figure G.4 External Timing Mode

You can choose one of these three modes with the three-position switch labeled "TRANSMIT TIMING SOURCE" on the interface module.

G.703 (2048 KBPS) MULTI-CLOCK AND STANDARD INTERFACES

Operation

IMPORTANT: The G.703 interface will only operate when the SX/12 External Transmit Timing Switch is in the "on" position.

The data rate on the SX/12 should be set to 2.048 MHz. Select the proper line coding with the dip switches located on the underside of the G.703 Multi-clock Interface module. The dip switches are described next.

Dip Switch 1

This dip switch sets the East and West line codes. Various line testing options are also available for the East and West channels.

Switch Position	Description
1	ETAO - East Transmit All Ones
2	ELL - East Local Loopback
3	ERL - East Remote Loopback
4	EC0 - East Code Select 0
5	EC1 - East Code Select 1
6	WTAO - West Transmit All Ones
7	WLL - West Local Loopback
8	WRL - West Remote Loopback
9	WC0 - West Code Select 0
10	WC1 - West Code Select 1

ETAO, WTAO - Setting to "1" causes continuous ones to be transmitted.
ELL, WLL - Setting to "1" routes the transmit clock and data from the SX/12 back into the SX/12 via the receive clock and data inputs of that port.
ERL, WRL - Setting to a "1" routes the recovered clock and receive data through the T1 driver of that port and back onto the line.
EC0, EC0, WC0, WC1 - Allow setting of code type for a particular channel as follows:

C0	C1	Code
0	0	AMI
0	1	B8ZS
1	0	B6ZS
1	1	HDB3

Optional Adapter Cables

ADP-BNC: 15 pin D connector to BNC adapter

pin 1 (TX Tip) to TX BNC center
pin 9 (TX Ring) to TX BNC shield
pin 3 (RX Tip) to RX BNC center
pin 11 (RX Ring) to RX BNC shield

ADP-TWX: 15 pin D connector to Twinax adapter

pin 1 (TX Tip) to TX Twinax lead 1
pin 9 (TX Ring) to TX Twinax lead 2
pin 2 (chassis ground) to TX Twinax shield
pin 3 (RX Tip) to RX Twinax lead 1
pin 11 (RX Ring) to RX Twinax lead 2
pin 4 (chassis ground) to RX Twinax shield

Specifications

Transmitter:

Output pulse amplitude: 2.37V (75 ohm coaxial cable setting)
3.0V (120 ohm twisted pair setting)

Complies with CCITT G.703 pulse shape for 2.048 MHz.

Receiver:

Sensitivity: -12dB (1.5 Vpp).

Allowable Consecutive Zeros before LOS: 160 - 190 (175 nominal)

Jitter tolerance: Better than 300 UIs at 6 Hz, 0.4 UIs 10 kHz to 100kHz.

Input impedance: selectable, 75 ohm (coaxial cable) or 120 ohms (twisted pair).

Transparent to G.703 framing.

Clock Generator Output:

TTL level into 50 ohms.

BNC female connector

2.048 MHz ±25 ppm

External Clock Input:

Input voltage: TTL levels

Input impedance: 50 ohms.

Input frequency: 2.048 MHz (jitter and frequency error can also be added)

TX, RX Connector:

Dual bantam connector

Network Connector:

15 pin female D connector

Pin	Signal
1	Send to network tip
9	Send to network ring
2	Chassis ground
3	Receive from network tip
11	Receive from network ring
4	Chassis ground

Interface Panel Indicators:

LOS - Loss Of Signal is lit when 175 consecutive zeros have been received. Indicator goes off when the received signal returns to 12.5% ones density, based on 4 ones out of 32 bit periods.

TX MON - Transmitter Monitor is lit if no signal is present on the transmitter tip and ring for 63 consecutive clock cycles.

CODE ERROR - Code Error is lit if a violation of the line coding scheme is detected.

CLK SLIP - Clock Slip is lit when the Elastic Buffer overflows or underflows. This will occur when the clocked data on the RCV line is not at the same nominal frequency as the internal or external source clock.

Switches:

The two toggle switch set receiver impedance of the East or West channel to 75 or 120 ohms. East and West channels are independently settable.

The three position switch selects the SX/12's transmit timing source. Source can be Internal, External, or Recovered.

G.703 Standard Interface

The G.703 Standard Interface Module is designed to convert between the TTL signals used within the SX/12 and signals complying with CCITT G.703 specification for 2.048 MHz signals. East and West dual bantam jacks and 15 pin D type connectors are provided for receive and transmit data. Adapters for BNC and Twinax connectors are also available. LED indicators provide line status information. A BNC type connector provides a TTL level clock source. Timing for the East and West-bound G.703 Data streams are generated by the external G.703 equipment.

The G.703 Interface Module has the following capabilities:

- East and West channels independently selectable for AMI, B8ZS, B6ZS, and HDB3 coding.
- Maximum range is greater than 1500 feet.
- Receiver sensitivity is -12dB.
- Receiver jitter tolerance is 300 UIs at 6 Hz to 0.4 UIs at 100 kHz.
- Interface is transparent to signal data framing.
- Toggle switches select 75 or 120 ohm receiver impedance for coaxial or twisted pair cables.
- Interface is transparent to G.703 framing.
- Interfaces with network equipment such as DACS, Channel Banks and DSX-1 cross connects.
- Interfaces with Customer Premises Equipment

Operation

IMPORTANT: The G.703 interface will only operate when the SX/12 External Transmit Timing Switch is in the "on" position.

The data rate on the SX/12 should be set to 2.048 MHz. Select the proper line coding with the dip switches on the G.703 interface module. The dip switches are described next.

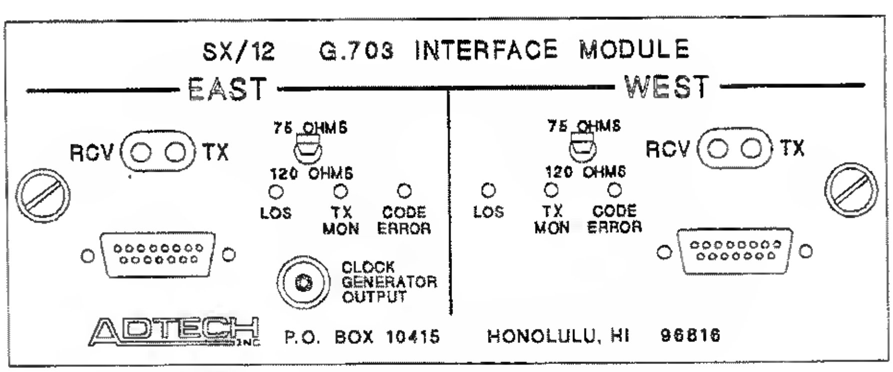

Figure G.5 G.703 (2.048 MHz) Standard Interface

This dip switch sets the East and West line codes. Various line testing options are also available for the East and West channels.

Switch Position	Description
1	ETAO - East Transmit All Ones
2	ELL - East Local Loopback
3	ERL - East Remote Loopback
4	EC0 - East Code Select 0
5	EC1 - East Code Select 1
6	WTAO - West Transmit All Ones
7	WLL - West Local Loopback
8	WRL - West Remote Loopback
9	WC0 - West Code Select 0
10	WC1 - West Code Select 1

ETAO, WTAO - Setting to "1" causes continuous ones to be transmitted.
ELL, WLL - Setting to "1" routes the transmit clock and data from the SX/12 back into the SX/12 via the receive clock and data inputs of that port.
ERL, WRL - Setting to a "1" routes the recovered clock and receive data through the T1 driver of that port and back onto the line.
EC0, EC0, WC0, WC1 - Allow setting of code type for a particular channel as follows:

C0	C1	Code
0	0	AMI
0	1	B8ZS
1	0	B6ZS
1	1	HDB3

Optional Adapter Cables

ADP-BNC: 15 pin D connector to BNC adapter

pin 1 (TX Tip) to TX BNC center
pin 9 (TX Ring) to TX BNC shield
pin 3 (RX Tip) to RX BNC center
pin 11 (RX Ring) to RX BNC shield

ADP-TWX: 15 pin D connector to Twinax adapter

pin 1 (TX Tip) to TX Twinax lead 1
pin 9 (TX Ring) to TX Twinax lead 2
pin 2 (chassis ground) to TX Twinax shield
pin 3 (RX Tip) to RX Twinax lead 1
pin 11 (RX Ring) to RX Twinax lead 2
pin 4 (chassis ground) to RX Twinax shield

G.703 (2048 KBPS) MULTI-CLOCK AND STANDARD INTERFACES

Specifications

Transmitter:

Output pulse amplitude: 2.37V (75 ohm coaxial cable setting)
3.0V (120 ohm twisted pair setting)

Complies with CCITT G.703 pulse shape for 2.048 MHz.

Receiver:

Sensitivity: -12dB (1.5 Vpp).

Allowable Consecutive Zeros before LOS: 160 - 190 (175 nominal)

Jitter tolerance: Better than 300 UIs at 6 Hz, 0.4 UIs 10 kHz to 100kHz.

Input impedance: selectable, 75 ohm (coaxial cable) or 120 ohms (twisted pair).

Transparent to G.703 framing.

Clock Generator Output:

TTL level into 50 ohms.

BNC female connector

TX, RX Connector:

Dual bantam connector

Network Connector:

15 pin female D connector

Pin	Signal
1	Send to network tip
9	Send to network ring
2	Chassis ground
3	Receive from network tip
11	Receive from network ring
4	Chassis ground

Interface Panel Indicators:

LOS - Loss Of Signal is lit when 175 consecutive zeros have been received. Indicator goes off when the received signal returns to 12.5% ones density, based on 4 ones out of 32 bit periods.

TX MON - Transmitter Monitor is lit if no signal is present on the transmitter tip and ring for 63 consecutive clock cycles.

CODE ERROR - Code Error is lit if a violation of the line coding scheme is detected.

Switches:

The two toggle switch set receiver impedance of the East or West channel to 75 or 120 ohms. East and West channels are independently settable.

Appendix H
IEEE-488 Remote Interface

Description

The IEEE-488 Remote Interface allows the SX/12 to be controlled remotely by an IEEE-488 controller. All operations that can be obtained hy pressing the keys on the front panel can also be obtained by using the SX/12 IEEE-488 device dependent commands. This appendix provides detailed information about each of the device dependent commands and how they are used to operate the SX/12. Refer to Chapter 1 for information on the various SX/12 functions and Chapter 4 for information concerning programming.

The SX/12 notifies the user of the IEEE-488 interface module's presence when the unit is powered up. The message "IEEE-488 Remote Interface Installed" should be display after the normal SX/12 sign-on message. If a problem with the interface is detected during power-up, an error message "INTERFACE MALFUNCTION" is also displayed. Pressing the [CLR] key will abort the remote interface and allow normal keyboard operation of the SX/12.

SX/12 IEEE-488 Interface Capabilities

The following IEEE-488 interface functions are implemented on the SX/12.

SERIAL POLLING - A service request is generated when certain error conditions occur. Performing a serial poll to the SX/12 will cause a status byte to be output with the following bits:

Bit 0(01H) = Command syntax error
Bit 1(02H) = Command timeout error
Bit 2(04H) = Download CRC error
Bit 6(40H) = Status valid

Bits 0-2 are only valid when bit 6 is set and should otherwise be ignored.

INTERFACE CLEAR - Aborts any pending input or output transmission and SX/12 function.

REMOTE/LOCAL/LOCAL LOCKOUT - Complete capability. Normal keyboard operation is possible whenever the SX/12 isn't processing a remote command. If local operation is not desirable, sending the IEEE Local Lockout command will disable the front panel keys until the IEEE Local command is sent.

DEVICE CLEAR - Resets the SX/12 to its "power-up" state.

GROUP EXECUTE TRIGGER - Used to continue a running SX/12 program that is waiting for a manual trigger.

SX/12 IEEE-488 Address

The default IEEE-488 address is 00. This address is retained in the battery backed memory when power is removed. To change the address do the following:

1. Press the [REMOTE] key.
2. Enter the new address.
3. Press the [ENTER] key to end the entry. Press the [CLR] key if an error was made to reenter the correction. The range of allowable addresses is 0 - 30.

SX/12 IEEE-488 Mnemonics

The IEEE-488 remote SX/12 commands have been implemented to closely resemble front panel key entry. Table H.1 lists the mnemonics for the SX/12 front panel keys. SX/12 functions accessed through the [OPTIONS] key on the front panel are accessed directly with the mnemonics listed in Table H.2 . The units on certain functions, selected by the [SELECT] key on the front panel, are accessed directly with the mnemonics listed in Table H.3 . Table H.4 lists additional remote commands that perform functions that are not possible from the SX/12 front panel.

With the exception of the binary upload and download commands, the remote function commands consist of ASCII representations of the alpha and numeric characters. Both upper case and lower case letters can be used interchangeably. All of the functions begin with a two character mnemonic and end with the CR LF (carriage return, line feed) terminator. Data keys are sent with the "0123456789" (numeric), "." (decimal point), "K" ($x10^3$), and "M" ($x10^6$) characters. Select options, used on certain functions are selected with the "F" (fixed), "R" (random), "B" (bits or bytes), "S" (milliseconds), and "T" (manual trigger) characters. The [ENTER] key, used extensively with front panel entries, is not required in the remote commands and is ignored if used. Table H.5 lists the keyboard mnemonics along with their proper syntax.

Multiple functions can be put on the same line when separated by delimiters, but the last function must end with the CR LF terminator. Three different delimiters are allowed: " " (space), "," (comma), and ";" (semi-colon).

i.e., "DL1K;DR1.544M;EE16;EW26;DW12;DE12;LE100BF;LW100BF;GE150F;GW150F(crlf)".

The binary upload and download commands allow binary data, such as the SX/12 parameter configuration, to be uploaded to and downloaded from the IEEE-488 controller. The upload file sent by the SX/12 in response to the upload command consist of: the download mnemonic, a two byte data count, the binary data, two CRC (cyclic redundancy check) bytes, and the EOI terminator. The embedded download mnemonic in the file allows downloading to the SX/12 to occur whenever the file is sent to it.

Table H.1 SX/12 Keyboard Mnemonics

Key	Mnemonic	Key	Mnemonic
[1]	1	[x10^3]	K
[2]	2	[ENTER]	E
[3]	3	[WEST RANDOM ERROR]	EW
[4]	4	[EAST RANDOM ERROR]	EE
[5]	5	[WEST BURST LENGTH]	LW
[6]	6	[EAST BURST LENGTH]	LE
[7]	7	[WEST GAP LENGTH]	GW
[8]	8	[EAST GAP LENGTH	GE
[9]	9	[WEST BURST DENSITY]	DW
[0]	0	[EAST BURST DENSITY]	DE
[.]	.	[DATA RATE]	DR
[CLR]	C	[DELAY]	DL
[x10^6]	M	[OPTIONS]	OP
[BW]	BW	[BW/E]	BB
[BE]	BE	[GOTO]	PG
[INS]	PI	[COPY]	PC
[DEL]	PD	[PCLR]	PE
[DUR]	PT	[STOP]	PS
[RUN]	PR	[PREV]	PB
[NEXT]	PF	[ERR]	ER
[E<->W]	CP		

Table H.2 SX/12 OPTIONS Mnemonics

Option	Mnemonic	Option	Mnemonic
[ASYNC MODE]	AS	[SYNC MODE]	SY
[BYPASS]	BP	[BYPASS EXIT]	BX
[KEYBOARD LOCKOUT]	KL	[KEYBOARD UNLOCK]	KX
[INWARD LOOPBACK]	IL	[OUTWARD LOOPBACK]	OL
[LOOPBACK EXIT]	LX	[SELF TEST]	ST
[PROGRAM EDIT MODE]	PM	[EXIT PROGRAM EDIT MODE]	PX

Table H.3 SX/12 Select Mnemonics

Select	Mnemonic	Select	Mnemonic
Fixed	F	Random or Repeat	R
Bits	B	Bytes	B
Milliseconds or Seconds	S	Manual Trigger	T

Table H.4 Non-Keyboard Mnemonics

Mnemonic	Description
(DC)	Download Configuration - Used to download a saved SX/12 parameter configuration. This function provides a quick method of programming the SX/12 parameters from a previously uploaded configuration file. Commonly used parameter setups can be saved using the IEEE-488 bus and restored when needed by downloading the uploaded file back to the SX/12. The 'DC' mnemonic is included in every uploaded configuration file and is sent to the SX/12 by sending an uploaded configuration file to the SX/12.
(DP)	Download Program - Used to download a saved SX/12 program. This function provides a quick method of restoring an SX/12 program from a previously uploaded program file. Commonly used programs can be saved using the IEEE-488 bus and restored when needed by downloading the uploaded program file back to the SX/12. The 'DP' mnemonic is included in every uploaded program file and is sent to the SX/12 by sending an uploaded program file to the SX/12.
ET	Execute Trigger - Used to continue the execution of a SX/12 program that is waiting on a manual trigger step. This command is an alternative to the IEEE-488 GROUP EXECUTE TRIGGER command.
ID	Send Identification - Used to remotely determine the SX/12 version and software revision.
RD	Read Current SX/12 Display - Used to upload the current SX/12 display.
RF	Read Frequency - Used to read the measured data clock frequency of the East channel.
UC	Upload Configuration - Used to upload the current SX/12 parameter configuration. This function provides a quick method of programming the SX/12 parameters. Commonly used parameter setups can be saved using the IEEE-488 bus and restored when needed by downloading the file to the SX/12.
UP	Upload Program - Used to upload the SX/12 program. This function allows SX/12 programs to be uploaded and saved on an IEEE-488 storage device. The programs can be quickly reloaded by downloading it to the SX/12.

Table H.5 SX/12 IEEE-488 Command Syntax

Mnemonic	Function	Description and Syntax
AS	Async Mode	Enters the SX/12 into its asynchronous mode for operation with asynchronous data. SYNTAX AS
BB	Burst Both	Triggers manual burst errors on the East and West channels. SYNTAX: BB
BE	Burst East	Triggers manual burst errors on the East channels. SYNTAX: BE
BP	Bypass	Enters the SX/12 into its bypass mode. SYNTAX: BP
BW	Burst West	Triggers manual burst errors on the West channels. SYNTAX: BW
BX	Bypass Exit	Enters the SX/12 into its normal mode. SYNTAX: BX
CPE	Copy to East	Copies the four error parameters from the West direction to the East direction of the channel. SYNTAX: CPE
CPW	Copy to West	Copies the four error parameters from the East direction to the West direction of the channel. SYNTAX: CPW

(DC)	Download Configuration	Restores the SX/12 parameter configuration from an uploaded configuration file SYNTAX: (DC...) Sending a previously uploaded binary configuration file consisting of 'DC', data count, binary data, CRC, and EOI terminator restores the SX/12's parameter configuration. The 'DC' mnemonic is already included in the configuration file from the upload process.
DE	Density East	Enters the burst density East parameter. SYNTAX: DE26 (density East = $2e^{-6}$ errors/bit)
DL	Delay	Enters the delay parameter. SYNTAX: DL1000B (delay = 1000 bytes) DL1.2KS (delay = 1200 ms.)
(DP)	Download Program	Restores the SX/12 program memory from an uploaded program file. SYNTAX: (DP...) Sending a previously uploaded binary program file consisting of 'DP', data count, binary data, CRC, and EOI terminator restores the SX/12's program memory. The 'DP' mnemonic is already included in the program file from the upload process.
DR	Data Rate	Enters the data rate parameter. SYNTAX: DR100 (data rate = 100 Hz) DR1K (data rate = 1000 Hz) DR1.544M (data rate = 1,544,000 Hz)
DW	Density West	Enters the burst density West parameter. SYNTAX: DW10 (density West = $1e^{0}$ errors/bit)
EE	Error East	Enters the random error East parameter. SYNTAX: EE19 (error East = $1e^{-9}$ errors/bit)

ER	Error On/Off	Alternately disables/enables the error generator for both East and West directions. SYNTAX: ER
ET	Execute Trigger	Continues a running SX/12 program that is waiting on the manual step trigger. SYNTAX: ET
EW	Error West	Enters the random error West parameter. SYNTAX: EW38 (error West = $3e^{-8}$ errors/bit)
GE	Gap East	Enters the burst gap length East parameter. SYNTAX: GET (manual trigger of the East error bursts) GE12345678F (gap length = 12,345,678 ms. , fixed length) GE1MR (gap length = 1,000,000 ms. , random length) GE2KF (gap length = 2,000 ms. , fixed length)
GW	Gap West	Enters the burst gap length West parameter SYNTAX: GWT (manual trigger of the West error bursts) GW1F (gap length = 1 ms. , fixed length) GW3.4MR (gap length = 3,400,000 ms. , random length) GW.5KR (gap length = 500 ms. , random length)
ID	Send Identification	Causes the SX/12 to send identification. SYNTAX: ID Returned value is an ASCII string containing the SX/12 model and software revision. i.e. , "SX/12-2 Data Channel Simulator Rev 2.00"
IL	Inward Loopback.	Enters the SX/12 into its inward loopback mode SYNTAX: IL

KL	Keyboard Lock	Enters the SX/12 into its keyboard lockout mode. SYNTAX: KL
KX	Keyboard Lock Exit	Enters the SX/12 into its normal mode. SYNTAX: KX
LE	Length East	Enters the burst length East parameter. SYNTAX: LE12345678BF (length East = 12,345,678 bits, fixed length) LE1.4MBR (length East = 1,400,000 bits, random length) LE2.1KSF (length East = 2,100 ms. , fixed length) LE10SR (length East = 10 ms. , random length)
LW	Length West	Enters the burst length West parameter. SYNTAX: LW1BF (length West = 1 bit, fixed length) LW3KBR (length West = 3,000 bits, random length) LW9999SF (length West = 9,999 ms. , fixed length) LW.2KSR (length West = 200 ms. , random length)
LX	Loopback Exit	Enters the SX/12 into its normal mode. SYNTAX: LX
OL	Outward Loopback.	Enters the SX/12 into its outward loopback mode SYNTAX: OL
PB	Program Back Step	Steps the SX/12 program backwards. (Used in the program edit mode) SYNTAX: PB
PC	Program Step Copy	Copies the parameters of the previous program step into the current program step. (Used in program edit mode) SYNTAX: PC

PD	Program Step Delete	Deletes the current program step. (Used in the program edit mode) SYNTAX: PD
PE	Program Erase	Erases the SX/12 program memory. SYNTAX: PE
PF	Program Forward Step	Steps the SX/12 program forward. (Used in the program edit mode) SYNTAX: PF
PG	Program Go To	Moves the SX/12 program to the specified step. (Used in the program edit mode) SYNTAX: PG12
PI	Program Step Insert	Inserts a new step into the SX/12 program at the current step number. (Used in the program edit mode) SYNTAX: PI
PM	Program Mode	Enters the SX/12 into its program edit mode. SYNTAX: PM
PR	Program Run	Starts the execution of the SX/12 program. SYNTAX: PR
PS	Program Stop	Stops the SX/12 program execution. SYNTAX: PS

PT	Program Step Time Duration	Enters the SX/12 step duration parameter. SYNTAX: PT1S (1 second step duration time) PT3.6KS (3,600 seconds step duration time) PT2MR (2,000,000 second step duration time, repeat program) PTT (Manual step trigger)
PX	Program Exit	Enters the SX/12 into its normal mode. SYNTAX: PX
RD	Read Display	Causes the SX/12 to send its current display. SYNTAX: RD Returned value is an ASCII string containing the information displayed on the LCD display and LED indicators. The string contains several CR LF characters and is terminated with the CR LF EOI IEEE-488 terminator. i.e., In the normal mode, the return string might be: "1.5440MHz 1E-8 100bF MANUAL 5E-1 1000ms 1E-8 100bF MANUAL 5E-1 Ext Timing OFF DTE Mode Freq MATCH " In the program edit mode, the returned string might be: "EDIT 10 Step Duration = 200 1.5440MHz 1E-8 100bF MANUAL 5E-1 1000ms 1E-8 100bF MANUAL 5E-1 Ext Timing OFF DTE Mode Freq MATCH " In the program run mode, the returned string might be: "RUN 12 Manual Trigger 1.5440MHz 1E-8 100bF MANUAL 5E-1 1000ms 1E-8 100bF MANUAL 5E-1 Ext Timing OFF DTE Mode Freq MATCH "

RF	Read Frequency	Causes the SX/12 to send the measured data clock frequency of the East channel. Returned values will be inaccurate for a few seconds after a rate change occurs. SYNTAX: RF Returned value is ASCII string containing the measured data rate. i.e. , "1.5440MHz"
ST	Self Test	Causes the SX/12 to enter its self test. Remote operation will not be possible until the tests are completed. SYNTAX: ST
SY	Synchronous Mode	Enters the SX/12 into its synchronous mode for operation with synchronous data. SYNTAX: SY
UC	Upload Configuration	Causes the SX/12 to send its current parameter configuration. SYNTAX: UC Returned value is a binary file consisting of "DC", data count, binary data, CRC, and EOI terminator. To download, just send this file to the SX/12.
UP	Upload Program	Causes the SX/12 to send the contents of its program memory. SYNTAX: UP Returned value is a binary file consisting of "DP", data count, binary data, CRC, and EOI terminator. To download, just send this file to the SX/12.

Extended T1 Simulation Option Mnemonics

Refer to Appendix K: Extended T1 Simulation Option, for the Extended T1 Simulation Option Mnemonics for the IEEE-488 Remote Interface.

IEEE-488 Mnemonic Quick Reference

Standard Settings

Mnemonic & syntax	Function
DL *number* [k/M][S/B]	Delay
DR *number* [k/M]	Data rate
EE *number (two digits)*	Random error rate East
EW *number (two digits)*	Random error rate West
SY	Synchronous mode
AS	Asyncronous mode

Burst Error Functions

Mnemonic & syntax	Function
DE *number (two digits)*	Burst density East
DW *number (two digits)*	Burst density West
LE *number* [k/M][b/S]	Burst length East
LW *number* [k/M][b/S]	Burst length West
GE *number* [k/M]	Gap length East
GW *number* [k/M]	Gap length West
GET	Gap length manual East
GWT	Gap length manual West
BE	Trigger burst error East
BW	Trigger burst error West
BB	Trigger burst on both East and West

Data Routing Modes

Mnemonic & syntax	Function
BP	Bypass mode
BX	Exit bypass mode
IL	Inward loopback mode
OL	Outward loop back mode
LX	Exit loopback modes

Programming Functions

Mnemonic & syntax	Function
PM	Program mode
PX	Exit program mode
PR	Run program
PS	Stop program
PI	Insert program step
PT *number* [R]	Step time = x seconds
PTT [R]	Step time = manual trigger
ET	Trigger program to continue
PF	Step program forward
PB	Step program backward
PG *number (1-99)*	Go to program step
PC	Copy previous step into current step
PD	Delete current step
PE	Erase entire program

Utilities

Mnemonic & syntax	Function
ID	Get SX12's identification
RD	Read LCD display
RF	Read clock frequency
ER	Error On/Off
CPE	Copy errors to East
CPW	Copy errors to West
UP	Upload current program
(DP)*(send file to SX/12)*	Download program
UC	Upload configuration
(DC)*(send file to SX/12)*	Download configuration
KL	keyboard lockout
KX	Release keyboard lockout
ST	Self test

Appendix I

G.703 (8448 kbps) Interface

Description

The G.703 Interface Module is designed to convert between the TTL signals used within the SX/12 and signals complying with CCITT G.703 specification for 8.448 Mbps signals. East and West dual BNC connectors are provided for receive and transmit data. The outer conductor of the transmit BNC connectors are connected to earth ground. Jumpers JU1 and JU2 on the circuit board have been provided to allow earth ground connections to the outer conductor of the receive BNC connectors. The LED indicator indicates the power-on condition.

The G.703 Interface Module has the following capabilities:

- Uses HDB3 line coding.
- Receiver sensitivity is -10dB.
- Interface is transparent to signal data framing.
- Interfaces with network equipment such as DACS and Channel Banks.
- Interfaces with Customer Premises Equipment

Operation

IMPORTANT: The G.703 interface will only operate when the SX/12 External Transmit Timing Switch is in the "on" position.

Proper operation of the SX/12 requires that its data rate be set to 8.448 MHz. The external transmit timing switch must be in the "on" position since the clock is recovered from the received data.

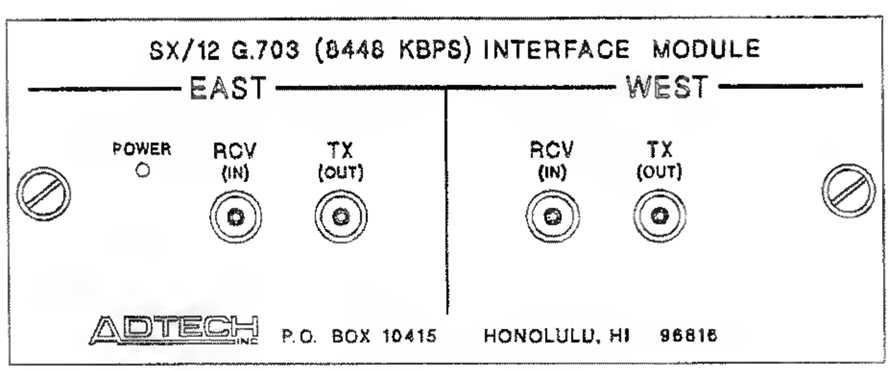

Figure I.1 G.703 (8.448 MHz) Interface

G.703 (8448 kbps) INTERFACE

Specifications

Transmitter:

Output pulse amplitude: 2.37V (75 ohm load)

Complies with CCITT G.703 pulse shape for 8.448 Mbps

Receiver:

Sensitivity: -10dB

Input impedance: 75 ohm

Transparent to G.703 framing

TX, RX Connector:

BNC connector with outside conductor of the transmit BNCs tied to earth ground. Optional grounding jumper straps for the receive BNCs have been provided to ground the outside conductor to earth ground.

Appendix J

RS-232-C Remote Interface

Description

The RS-232-C Remote Interface allows the SX/12 to be controlled remotely by an RS-232 terminal or any computer that has a RS-232 port and communications software. For IBM compatible PCs, a screen oriented SX/12 program called 'SX/PC' is provided with the interface.

All operations that can be obtained by pressing keys on the front panel can also be obtained by using the SX/12 remote commands. This appendix provides detailed information about each of the commands and how they are used to operate the SX/12. Refer to Chapter 1 for information on the various SX/12 functions and Chapter 4 for information concerning programming.

The SX/12 notifies the user of the RS-232 Remote Interface module's presence when the unit is powered up. The message 'RS-232 Remote Interface Installed' should be displayed after the normal SX/12 sign-on message. If a problem with the interface is detected during power-up, an error message 'INTERFACE MALFUNCTION' is also displayed. Pressing the [CLR] key will abort the remote interface and allow normal keyboard operation of the SX/12.

RS-232 Port Configuration

The baud rate, number of stop bits and parity must be set to match those of the controlling device. The number of data bits is always 8 bits and must be set as such on the controlling device. The SX/12 RS-232 port settings are retained in the battery-backed memory when power is removed.

To modify the RS-232 port settings, do the following:

1. Press the [REMOTE] key.
2. Press the [SELECT] key to select the baud rate.
3. Press the [ENTER] key to enter the baud rate selection. The blinking cursor will move to the stop bit selection.
4. Press the [SELECT] key to select the number of stop bits.
5. Press the [ENTER] key to enter the parity selection. The blinking cursor will move to the parity selection.
6. Press the [SELECT] key to select the type of parity.
7. Press the [ENTER] key to enter the parity selection and return to the normal display.

SX/12 RS-232 Remote Command Mnemonics

The RS-232 remote commands have been implemented to closely resemble front panel key entry. Table J.1 lists the mnemonics for the SX/12 front panel keys. SX/12 functions accessed through the [OPTIONS] key on the front panel are accessed directly with the mnemonics listed in Table J.2 . The units on certain functions, selected by the [SELECT] key on the front panel, are accessed directly with the mnemonics listed in Table J.3 . Table J.4 lists additional remote commands that perform functions that are not possible from the SX/12 front panel.

With the exception of the binary upload and download commands, the remote commands consist of ASCII representations of the alpha and numeric characters. Both upper case and lower case letters can be used interchangeably. All of the commands begin with a one or two character mnemonic and end with the CR LF (carriage return, line feed) terminator. Data keys are sent with the '0123456789' (numeric), '.' (decimal point), 'K' (x103), and 'M' (x106) characters. Select options, used on certain functions are selected with the 'F' (fixed), 'R' (random), 'B' (bits or bytes), 'S' (milliseconds), and 'T' (manual trigger) characters. The [ENTER] key 'E', used extensively with front panel entries, is not required in the remote commands and is ignored if used. Table J.5 lists all of the remote commands along with command descriptions and syntax examples.

Multiple functions can be put on the same line when separated by delimiters, but the last function must end with the CR LF terminator. Three different delimiters are allowed: ' ' (space), ',' (comma), and ';' (semi-colon).

i.e., 'DL1K;DR1.544M;EE16;EW26;DW12;DE12;LE100BF;LW100BF;GE150F;GW150F(crlf)'.

The binary upload and download commands allow binary data, such as the SX/12 parameter configuration, to be uploaded to and downloaded from the RS-232 controller. The upload file sent by the SX/12 in response to the upload command consist of: the download mnemonic, a two byte data count, the binary data, and two CRC (cyclic redundancy check) bytes. The embedded download mnemonic in the file allows downloading to the SX/12 to occur whenever the file is sent to it.

The SX/12 returns a response character after receiving each command. The following are the possible response characters and their meanings:

' * ' Command received and processed.

' ? ' Syntax error in the received command.

' > ' Timeout occurred during the processing of the command.

' ! ' CRC error occurred during a program or configuration download.

The X-ON and X-OFF messages are supported in the following RS-232 Remote Commands:
RD, UC, and UP. To start or stop transmission, send the X-ON or X-OFF message.

Table J.1 SX/12 Keyboard Mnemonics

Key	Mnemonic	Key	Mnemonic
[1]	1	[x103]	K
[2]	2	[ENTER]	E
[3]	3	[WEST RANDOM ERROR]	EW
[4]	4	[EAST RANDOM ERROR]	EE
[5]	5	[WEST BURST LENGTH]	LW
[6]	6	[EAST BURST LENGTH]	LE
[7]	7	[WEST GAP LENGTH]	GW
[8]	8	[EAST GAP LENGTH	GE
[9]	9	[WEST BURST DENSITY]	DW
[0]	0	[EAST BURST DENSITY]	DE
[.]	.	[DATA RATE]	DR
[CLR]	C	[DELAY]	DL
[x106]	M	[OPTIONS]	OP
[BW]	BW	[BW/E]	BB
[BE]	BE	[GOTO]	PG
[INS]	PI	[COPY]	PC
[DEL]	PD	[PCLR]	PE
[DUR]	PT	[STOP]	PS
[RUN]	PR	[PREV]	PB
[NEXT]	PF	[ERR]	ER
[E<->W]	CP		

Table J.2 SX/12 OPTIONS Mnemonics

Option	Mnemonic	Option	Mnemonic
[ASYNC MODE]	AS	[SYNC MODE]	SY
[BYPASS]	BP	[BYPASS EXIT]	BX
[KEYBOARD LOCKOUT]	KL	[KEYBOARD UNLOCK]	KX
[INWARD LOOPBACK]	IL	[OUTWARD LOOPBACK]	OL
[LOOPBACK EXIT]	LX	[SELF TEST]	ST
[PROGRAM EDIT MODE]	PM	[EXIT PROGRAM EDIT MODE]	PX

Table J.3 SX/12 Select Mnemonics

Select	Mnemonic	Select	Mnemonic
Fixed	F	Random or Repeat	R
Bits	B	Bytes	B
Milliseconds or Seconds	S	Manual Trigger	T

Table J.4 Non-Keyboard Mnemonics

Mnemonic	Description
(DC)	Download Configuration - Used to download a saved SX/12 parameter configuration. This function provides a quick method of programming the SX/12 parameters from a previously uploaded configuration file. Commonly used parameter setups can be saved using the RS-232 port and restored when needed by downloading the uploaded file back to the SX/12. The 'DC' mnemonic is included in every uploaded configuration file and is sent to the SX/12 by sending an uploaded configuration file to the SX/12.
(DP)	Download Program - Used to download a saved SX/12 program. This function provides a quick method of restoring an SX/12 program from a previously uploaded program file. Commonly used programs can be saved using the RS-232 port and restored when needed by downloading the uploaded program file back to the SX/12. The 'DP' mnemonic is included in every uploaded program file and is sent to the SX/12 by sending an uploaded program file to the SX/12.
ET	Execute Trigger - Used to continue the execution of a SX/12 program that is waiting on a manual trigger step.
LL	Local Lockout - Used to remotely disable the SX/12 keyboard.
LO	Local Lockout Off - Used to remotely re-enable the SX/12 keyboard.
ID	Send Identification - Used to remotely determine the SX/12 version and software revision.
RD	Read Current SX/12 Display - Used to upload the current SX/12 display.
RF	Read Frequency - Used to read the measured data clock frequency of the East channel.
RS	Reset - Used to reset the SX/12 back to its power-on state.
UC	Upload Configuration - Used to upload the current SX/12 parameter configuration. This function provides a quick method of programming the SX/12 parameters. Commonly used parameter setups can be saved by the RS-232 controller and restored when needed by downloading the file to the SX/12.
UP	Upload Program - Used to upload the SX/12 program. This function allows SX/12 programs to be uploaded and saved on the RS-232 controller. The programs can be quickly reloaded by downloading it to the SX/12.
I	Interface Clear - Used to reset the RS-232 interface in order to regain control.

Table J.5 SX/12 RS-232 Command Syntax

Mnemonic	Function	Description and Syntax
AS	Async Mode	Enters the SX/12 into its asynchronous mode for operation with asynchronous data. SYNTAX AS
BB	Burst Both	Triggers manual burst errors on the East and West channels. SYNTAX: BB
BE	Burst East	Triggers manual burst errors on the East channels. SYNTAX: BE
BP	Bypass	Enters the SX/12 into its bypass mode. SYNTAX: BP
BW	Burst West	Triggers manual burst errors on the West channels. SYNTAX: BW
BX	Bypass Exit	Enters the SX/12 into its normal mode. SYNTAX: BX
CPE	Copy to East	Copies the four error parameters from the West direction to the East direction of the channel. SYNTAX: CPE
CPW	Copy to West	Copies the four error parameters from the East direction to the West direction of the channel. SYNTAX: CPW

(DC)	Download Configuration	Restores the SX/12 parameter configuration from an uploaded configuration file SYNTAX: (DC...) Sending a previously uploaded binary configuration file consisting of 'DC', data count, binary data, and CRC terminator restores the SX/12's parameter configuration. The 'DC' mnemonic is already included in the configuration file from the upload process.
DE	Density East	Enters the burst density East parameter. SYNTAX: DE26 (density East = 2e-6 errors/bit)
DL	Delay	Enters the delay parameter. SYNTAX: DL1000B (delay = 1000 bytes) DL1.2KS (delay = 1200 ms.)
(DP)	Download Program	Restores the SX/12 program memory from an uploaded program file. SYNTAX: (DP...) Sending a previously uploaded binary program file consisting of 'DP', data count, binary data, and CRC terminator restores the SX/12's program memory. The 'DP' mnemonic is already included in the program file from the upload process.
DR	Data Rate	Enters the data rate parameter. SYNTAX: DR100 (data rate = 100 Hz) DR1K (data rate = 1000 Hz) DR1.544M (data rate = 1,544,000 Hz)
DW	Density West	Enters the burst density West parameter. SYNTAX: DW10 (density West = 1e0 errors/bit)
EE	Error East	Enters the random error East parameter. SYNTAX: EE19 (error East = 1e-9 errors/bit)

ER	Error On/Off	Alternately disables/enables the error generator for both East and West directions. SYNTAX: ER
ET	Execute Trigger	Continues a running SX/12 program that is waiting on the manual step trigger. SYNTAX: ET
EW	Error West	Enters the random error West parameter. SYNTAX: EW38 (error West = 3e-8 errors/bit)
GE	Gap East	Enters the burst gap length East parameter. SYNTAX: GET (manual trigger of the East error bursts) GE12345678F (gap length = 12,345,678 ms. , fixed length) GE1MR (gap length = 1,000,000 ms. , random length) GE2KF (gap length = 2,000 ms. , fixed length)
GW	Gap West	Enters the burst gap length West parameter SYNTAX: GWT (manual trigger of the West error bursts) GW1F (gap length = 1 ms. , fixed length) GW3.4MR (gap length = 3,400,000 ms. , random length) GW.5KR (gap length = 500 ms. , random length)
ID	Send Indentification	Causes the SX/12 to send identification. The string is terminated by the ' * ' character. SYNTAX: Returned value is an ASCII string containing the SX/12 model and software revision. i.e. , 'SX/12-2 Data Channel Simulator Rev 2.00'
IL	Inward Loopback.	Enters the SX/12 into its inward loopback mode SYNTAX: IL
KL	Keyboard Lock	Enters the SX/12 into its keyboard lockout mode. SYNTAX: KL

KX	Keyboard Lock Exit	Enters the SX/12 into its normal mode. SYNTAX: KX
LE	Length East	Enters the burst length East parameter. SYNTAX: LE12345678BF (length East = 12,345,678 bits, fixed length) LE1.4MBR (length East = 1,400,000 bits, random length) LE2.1KSF (length East = 2,100 ms. , fixed length) LE10SR (length East = 10 ms. , random length)
LL	Local Lockout	Disables the SX/12 keyboard. SYNTAX: LL
LO	Local Lockout Off	Re-enables the SX/12 keyboard. SYNTAX: LO
LW	Length West	Enters the burst length West parameter. SYNTAX: LW1BF (length West = 1 bit, fixed length) LW3KBR (length West = 3,000 bits, random length) LW9999SF (length West = 9,999 ms. , fixed length) LW.2KSR (length West = 200 ms. , random length)
LX	Loopback Exit	Enters the SX/12 into its normal mode. SYNTAX: LX
OL	Outward Loopback.	Enters the SX/12 into its outward loopback mode SYNTAX: OL
PB	Program Back Step	Steps the SX/12 program backwards. (Used in the program edit mode) SYNTAX: PB

PC	Program Step Copy	Copies the parameters of the previous program step into the current program step. (Used in program edit mode) SYNTAX: PC
PD	Program Step Delete	Deletes the current program step. (Used in the program edit mode) SYNTAX: PD
PE	Program Erase	Erases the SX/12 program memory. (Used in the program edit mode) SYNTAX: PE
PF	Program Forward Step	Steps the SX/12 program forward. (Used in the program edit mode) SYNTAX: PF
PG	Program Go To	Moves the SX/12 program to the specified step. (Used in the program edit mode) SYNTAX: PG12 (displays program step 12 as the current program step)
PI	Program Step Insert	Inserts a new step into the SX/12 program at the current step number. (Used in the program edit mode) SYNTAX: PI
PM	Program Mode	Enters the SX/12 into its program edit mode. SYNTAX: PM
PR	Program Run	Starts the execution of the SX/12 program. SYNTAX: PR
PS	Program Stop	Stops the SX/12 program execution. SYNTAX: PS

PT	Program Step Time Duration	Enters the SX/12 step duration parameter. (Used in the program edit mode) SYNTAX: PT1S (1 second step duration time) PT3.6KS (3,600 seconds step duration time) PT2MR (2,000,000 second step duration time, repeat program) PTT (Manual step trigger)
PX	Program Exit	Enters the SX/12 into its normal mode. SYNTAX: PX
RD	Read Display	Causes the SX/12 to send its current display. SYNTAX: RD

Returned value is an ASCII string containing the information displayed on the LCD display and LED indicators. The string contains several CR LF characters and is terminated with the CR LF ' * '. The RD command supports the X-ON and X-OFF messages.

i.e.,
In the normal mode, the return string might be:

```
'1.5440MHz  1E-8   100bF   MANUAL    5E-1
 1000ms     1E-8   100bF   MANUAL    5E-1
 Ext Timing OFF    DTE Mode     Freq MATCH '
```

In the program edit mode, the returned string might be:

```
'EDIT   10         Step Duration = 200
 1.5440MHz 1E-8    100bF   MANUAL    5E-1
 1000ms    1E-8    100bF   MANUAL    5E-1
 Ext Timing OFF    DTE Mode     Freq MATCH '
```

In the program run mode, the returned string might be:

```
'RUN    12         Manual Trigger
 1.5440MHz 1E-8    100bF   MANUAL    5E-1
 1000ms    1E-8    100bF   MANUAL    5E-1
 Ext Timing OFF    DTE Mode     Freq MATCH '
```

RF	Read Frequency	Causes the SX/12 to send the measured data clock frequency of the East channel. Returned values will be inaccurate for a few seconds after a rate change occurs. The string is terminated by the ' * ' character. SYNTAX: RF Returned value is ASCII string containing the measured data rate. i.e. , '1.5440MHz'
RS	Reset	Resets the SX/12 to its power-on state. SYNTAX: RS
ST	Self Test	Causes the SX/12 to enter its self test. Remote operation will not be possible until the tests are completed. SYNTAX: ST
SY	Synchronous Mode	Enters the SX/12 into its synchronous mode for operation with synchronous data. SYNTAX: SY
UC	Upload Configuration	Causes the SX/12 to send its current parameter configuration. SYNTAX: UC Returned value is a binary file consisting of 'DC', data count, binary data, CRC, and ' * ' terminator. To download, just send this file to the SX/12. The UC command supports the X-ON and X-OFF messages.
UP	Upload Program	Causes the SX/12 to send the contents of its program memory. SYNTAX: UP Returned value is a binary file consisting of 'DP', data count, binary data, CRC, and ' * 'terminator. To download, just send this file to the SX/12. The UP command supports the X-ON and X-OFF messages.

Extended T1 Simulation Option Mnemonics

Refer to Appendix K: Extended T1 Simulation Option, for the Extended T1 Simulation Option Mnemonics for the RS-232-C Remote Interface.

SX/PC Remote Control Program

SX/PC is a program that allows the SX/12 to be remotely controlled from an IBM PC/AT or compatible computer. It requires a free RS-232 port on the computer and the RS-232-C Remote Interface Option on the SX/12.

Installation and Setup

SX/PC comes on a 5 inch, low density floppy diskette. It contains a single file called 'SXPC.EXE.' To install the program onto a hard disk, simply copy 'SXPC.EXE' into the desired directory.

When running the program for the first time, the user must first enter the 'Setup' menu to set the baud rate, parity, and number of stop bits to match the line settings of the SX/12 (the 'REMOTE' key on the SX/12 displays the SX/12's line settings and allows changes to be made). The next step is to enter the number of the communications port that the RS-232-C Remote Interface is connected to. The user then has a choice of various background and text colors to choose from. Finally, by entering 'Y' (Yes) at the 'Save Information?' prompt, the above parameters will be saved to a file called 'SXPC.CFG' and will be automatically setup the next time SX/PC is run. The setup parameters can be changed at any time by reentering the 'Setup' menu.

Operation

Mode Menu

After the setup has been completed, enter the 'Mode' menu. This menu gives the user a choice of three different control modes: **Normal, On Line Program,** or **Terminal.**

The **Normal** mode allows the user to control all of the normal SX/12 parameters such as delay, data rate, and error settings. The computer screen displays the SX/12's current parameter settings in a format similar to the SX/12's LCD front panel display. The highlighted box on the screen is moved from one parameter to the next by using the computer's cursor keys. To edit a parameter, press the space bar, then type in the new parameter value while following the syntax displayed at the bottom of the screen, and press the Enter key.

The **On Line Program** mode allows the user to control the SX/12 in its program mode. Furthermore, three consecutive program steps are shown simultaneously. The cursor keys are used to move between parameters and to scroll between program steps. To edit a parameter, first press the space bar, then type in the new parameter value while following the syntax displayed at the bottom of the screen, and press the Enter key.

The **Terminal** mode allows the user to control the SX/12 by typing in the command mnemonics directly as defined in the beginning of this appendix. This allows the user to link commands together on a single line so that they will take effect together. It also allows

additional commands from special SX/12 options, such as the Extended T1 Simulation Option, to be entered.

The upload and download commands are special cases in the Terminal mode. To use these commands, type the mnemonic followed by the filename which will store (upload) or provide (download) data for the SX/12. Do not use file extensions in the filename. SX/PC automatically adds the extension '.PG1' to all program files and the extension '.CG1' to all configuration files when they are uploaded or downloaded.

Options Menu

The 'Options' menu has three possible functions: toggle the SX/12 between synchronous and asynchronous mode, reset the SX/12, and erase the program on the SX/12. You may only switch between synchronous and asynchronous in the Normal mode and the erase program option is only available in the On Line Program mode. You may reset the SX/12 from any mode.

File Menu

The 'File' menu allows you to upload and download programs and configurations. When specifying a filename do not use file extensions. SX/PC automatically adds the extension '.PG1' to all program files and the extension '.CG1' to all configuration files when they are uploaded or downloaded.

RS-232 Mnemonic Quick Reference

Standard Settings

Mnemonic & syntax	Function
DL *number* [k/M][S/B]	Delay
DR *number* [k/M]	Data rate
EE *number (two digits)*	Random error rate East
EW *number (two digits)*	Random error rate West
SY	Synchronous mode
AS	Asyncronous mode

Burst Error Functions

DE *number (two digits)*	Burst density East
DW *number (two digits)*	Burst density West
LE *number* [k/M][b/S]	Burst length East
LW *number* [k/M][b/S]	Burst length West
GE *number* [k/M]	Gap length East
GW *number* [k/M]	Gap length West
GET	Gap length manual East
GWT	Gap length manual West
BE	Trigger burst error East
BW	Trigger burst error West
BB	Trigger burst on both East and West

Data Routing Modes

BP	Bypass mode
BX	Exit bypass mode
IL	Inward loopback mode
OL	Outward loop back mode
LX	Exit loopback modes

Programming Functions

Mnemonic & syntax	Function
PM	Program mode
PX	Exit program mode
PR	Run program
PS	Stop program
PI	Insert program step
PT *number* [R]	Step time = x seconds
PTT [R]	Step time = man. trigger
ET	Trigger program to continue
PF	Step program forward
PB	Step program backward
PG *number (1-99)*	Go to program step
PC	Copy previous step
PD	Delete current step
PE	Erase entire program

Utilities_

ER	Error On/Off
CPE	Copy errors to East
CPW	Copy errors to West
ID	Get SX12's identification
RD	Read LCD display
RF	Read clock frequency
UP	Upload current program
DP *(send file to SX/12)*	Download program
UC	Upload configuration
DC *(send file to SX/12)*	Download configuration
KL	keyboard lockout
KX	Release keyboard lockout
LL	Disallow local control
LO	Allow local control
ST	Self test

Appendix K
Extended T1/E1 Simulation Option

Description

The Extended T1/E1 Simulation Option is a factory installed hardware option for the SX/12. It provides the SX/12 with additional delay and error simulation capabilities for North American T1 or CEPT E1 data streams in a variety of framing formats. Once installed, it can be enabled or disabled from the SX/12's front panel keypad. When enabled, it allows the user to add variable delays to DS0s or time slots in the T1 or E1 data stream. It also allows errors to be targeted at specific time slots and overhead bits in the T1 or E1 multiframe, such as signaling, framing, alarm, and CRC bits.

Time Slot Delays

Without the Extended T1/E1 Simulation Option installed and enabled, the SX/12's main channel delay (entered on the main channel parameter screen) is applied to the entire T1 or E1 data stream. All framing bits and overhead bits as well as all of the DS0s/time slots will experience the same main channel delay.

With the Extended T1/E1 Simulation Option installed and enabled, the delay applied to each of the DS0s/time slots becomes independently selectable from one of two available sets of delay values while the framing and overhead bits continue to experience the normal main channel delay. Each of the DS0s/time slots can be set to experience any of the delays in the current set of available delays. These available delays are referred to as delay taps.

Depending on which of two modes is selected, there are either ten or nine delay taps available that can be applied to each DS0/time slot. These delay taps cannot have their delay times set to randomly programmed values. Instead, the delays are determined by three entered parameters that are combined with a set of formulas to determine the actual delay taps available. The first parameter is a Single Group or Double Group delay mode selection. Referring to table K.1, you will see that in the Single Group mode, all but one of the ten available delay taps are in a group referenced to the main channel delay. Delay tap 0 provides no delay to any time slots assigned to it while the delay times provided by delay taps 1 through 9 are determined by the main channel delay and a tap interval parameter according to the formulas in the table. This mode is most useful where all of the channels are traveling the same basic transmission path, but there might be some small variation between the individual DS0/time slot delays due to switching and cross-connect equipment. Delay numbers 1 through 9 could be assigned to various time slots to simulate this situation. Delay number 0 could be used when there is a large delay difference between some of the time slots. In that case, one or more time slots could be assigned to delay 0 while the others would be assigned to delay taps 1 through 9. The default time slot delay assignment when you first enter the option is delay tap 1 (the main channel delay) for all time slots, which is what occurs when the option is disabled.

Referring to table K.1, the Double Group mode provides nine delay taps in two groups. The first group are delay taps 0 to 3 which are referenced to no delay while the second group is made up of delay taps 4 through 8 which are referenced to the main channel delay. These two delay tap groups can simulate two very different transmission paths for the time slots, each of which has some variation in the delays experienced by individual time slots traveling that path. For example, some of the time slots could be over a satellite path while the others may take a terrestrial path. For each of the paths, there might be small variations in time slot delay due to switching equipment. The same parameters used in the single group mode (main channel delay and tap interval) determine the tap delays in the double group mode. The default tap assignment for all time slots in the double group mode is delay tap 4 (the main channel delay).

Single Group Mode		Double Group Mode	
Delay Tap	Time Slot Delay Setting	Delay Tap	Time Slot Delay Setting
0	No Delay	0	No Delay
1	Channel Delay	1	No Delay+Tap Interval x 1
2	Channel Delay+Tap Interval x 1	2	No Delay+Tap Interval x 2
3	Channel Delay+Tap Interval x 2	3	No Delay+Tap Interval x 3
4	Channel Delay+Tap Interval x 3	4	Channel Delay
5	Channel Delay+Tap Interval x 4	5	Channel Delay+Tap Interval x 1
6	Channel Delay+Tap Interval x 5	6	Channel Delay+Tap Interval x 2
7	Channel Delay+Tap Interval x 6	7	Channel Delay+Tap Interval x 3
8	Channel Delay+Tap Interval x 7	8	Channel Delay+Tap Interval x 4
9	Channel Delay+Tap Interval x 8	9	Not Assigned

Table K.1 DS0/Time Slot Delay Taps in Single and Double Group modes

For either mode, the main channel delay can be set to any valid channel delay value in milliseconds or frames. The main channel delay is always applied to the framing bits of the data stream. The delay applied to the time slots is dependent on the delay tap they are assigned to as defined in table K.1.

The tap interval parameter can be set in either frames or milliseconds from a minimum of one frame or one millisecond up to a maximum of 128 frames or 16 milliseconds. When using a tap interval value in frames, each frame of delay represents a one byte delay (equivalent to 0.125 milliseconds) for that time slot. A millisecond tap interval represents an eight frame delay which is eight bytes of delay for each time slot.

Formats of T1 and E1 streams that use signaling put additional constraints on the values of the tap interval and the main channel delay parameters. Signaling bits are carried in the time slots of these streams. For proper functioning of the downstream equipment, these signaling bits must be delayed by times that are a multiple of a multiframe length or they will be moved to the wrong location in another multiframe, upsetting signaling. For T1 streams that use in-band signaling, the main delay and the tap interval must be a multiple of 3ms (or 24 frames for ESF, 12 frames for D3/D4 if set in frames) which is the length of a multiframe, insuring that the signaling bits end up in the same position in another multiframe. For E1 streams that use in-band signaling, the main channel delay and the tap interval must be a multiple of 2ms (or 16 frames) which is the length of an E1 multiframe, insuring that the signaling bits end up in the same position in another E1 multiframe.

Error Targeting

The error targeting function provided by this option permits any of six available error types to be targeted at any selected overhead bits, data bits, or time slots in a multiframe. The six error types include random errors, random ones, random zeros, or forced errors, forced ones, or forced zeros. The bits selected to receive random error types will have their error probabilities determined by the SX/12's error parameters. These parameters include the random error rate as well as the burst error density, burst length, and gap length. The bits selected to receive forced errors will be in error in every multiframe selected to receive errors. Unselected bits and multiframes not selected to receive targeted errors will not receive any errors.

The error targeting function operates in either of two modes. The Continuous mode injects the targeted errors into every multiframe. Those bits targeted to receive random errors will receive errors in each multiframe where they coincide with error events from either the random or burst error generators. Those bits targeted to receive forced errors will have errors inserted in those bit positions in every multiframe. The second mode is the Manual Multiframe Burst mode. In this mode single multiframes are manually selected to receive errors by pressing one of the hurst error injection keys. The [BW], [BW/E], or [BE] keys select a multiframe on the

West, both, or East directions of the channel to receive targeted errors. These keys do not trigger the burst error generator when operating in this mode if the gap length is set to manual.

The bits that are selectable for targeting depend on the framing format selected. In general, any of the overhead bits or data bits in a multiframe can be targeted in any combination. Overhead bits may include framing, multiframe sync, signaling, CRC, terminal, data link, and alarm bits. Data bits can be selected either by individual bits or by time slots by choosing one of two variations of each available framing format. Individual data bit selection is available by selecting the clear channel version of the desired framing format. This gives you the most control over data bits to be targeted. The channelized versions of the formats permit errors to be targeted by time slots and time slot bits, simplifying targeting bit selection when a set of bits in one or more time slots are to receive errors. In all cases, the default targeting status when a new frame format is selected is no bits or time slots targeted.

General Information

The bit error targeting and the time slot delay assignments for the East and West channels of the SX/12 are completely independent and can be individually programmed. If both time slot delays and error targeting are used, delay is performed first, the CRC, if any, is recalculated and then errors are injected in the selected positions of the resulting data stream. All of the Extended T1/E1 delay and error parameters are stored in the SX/12's battery-backed memory for retention when the SX/12 is powered-down. The SX/12 also remembers if the Extended T1/E1 Simulation Option was enabled during its last session and will keep the option enabled the next time it is powered-up.

Data Formats Supported by the Extended T1/E1 Simulation Option

The Extended T1/E1 Simulation Option supports the following formatted data streams:

Format	Physical Line Type	Description
E1-framed	[G.703(2.048 Mbps)]	G.703 using two frame structure-no multiframe. Data bits targeted by channel time slot.
E1-framed clear channel	[G.703(2.048 Mbps)]	G.703 using two frame structure-no multiframe. Data bits targeted individually.
E1-multiframed/ signaling	[G.703(2.048 Mbps)]	G.703 using time slot 16 multiframe with signaling. Data bits targeted by channel time slot.
E1-multiframed/ clear channel	[G.703(2.048 Mbps)]	G.703 using time slot 16 multiframe with signaling. Data bits targeted individually.
E1-CRC4 no signaling	[G.703(2.048 Mbps)]	G.703 using CRC4 multiframe without signaling. Data bits targeted by channel time slot.
E1-CRC4 with signaling	[G.703(2.048 Mbps)]	G.703 using CRC4 multiframe with signaling. Data bits targeted by channel time slot.
E1-CRC4 clear channel	[G.703(2.048 Mbps)]	G.703 using CRC4 multiframe without signaling. Data bits targeted individually.
T1-ESF no signaling	[DS1(1.544 Mbps)]	T1 extended superframe structure without signaling. Data bits targeted by DS0 time slot.
T1-ESF with signaling	[DS1(1.544 Mbps)]	T1 extended superframe structure with signaling. Data bits targeted by DS0 time slot.
T1-ESF clear channel	[DS1(1.544 Mbps)]	T1 extended superframe structure without signaling. Data bits targeted individually.
T1-D3/D4 no signaling	[DS1(1.544 Mbps)]	T1 superframe multiframe structure without signaling. Data bits targeted by DS0 time slot.
T1-D3/D4 with signaling	[DS1(1.544 Mbps)]	T1 superframe multiframe structure with signaling. Data bits targeted by DS0 time slot.
T1-D3/D4 clear channel	[DS1(1.544 Mbps)]	T1 superframe multiframe structure without signaling. Data bits targeted individually.

Targetable Bits in E1-Framed Format

When set up for the E1-framed format (G.703(2.048 Mbps) with two frame/no multiframe structure), errors can be targeted to the following bits/time slots in the frame structure:

Bit To Target (Number of targetable bits)

Frame alignment (F) bits (16)

Data time slots (31) (selected by time slots and time slot bit mask)

This format is intended for channelized applications of basic E1.

Targetable Bits in E1-Framed Clear Channel Format

When set up for the E1-framed clear channel format (G.703(2.048 Mbps) with two frame/no multiframe structure), errors can be targeted to the following bits in the frame structure:

Bit To Target (Number of targetable bits)

Frame alignment (F) bits (16)

Data bits (496) (bits can be selected individually)

This format is intended for clear channel (unchannelized) applications of basic E1. Numbering of the data bits for error targeting into a multiframe of this format is bits 1-248 for frame 0 and bits 249-496 for frame 1.

Targetable Bits in E1-Multiframed / Signaling Format

When set up for the E1-multiframed/signaling format (G.703(2.048 Mbps) with time slot-16 multiframe structure with signaling), errors can be targeted to the following bits in the frame structure:

Bit To Target (Number of targetable bits)

Frame alignment (F) bits (128)

Multiframe sync bits (4)

Alarm/Spare (xyxx) bits (4)

Time slot signaling (abcd) bits (120)

Data time slots (30) (selected by time slots and time slot bit mask)

This format is intended for channelized applications of multiframe E1.

Targetable Bits in E1-Multiframed/Clear Channel Format

When set up for the E1-multiframed clear channel format (G.703(2.048 Mbps) with time slot-16 multiframe structure), errors can be targeted to the following bits in the frame structure:

Bit To Target (Number of targetable bits)

Frame alignment (F) bits (128)

Multiframe sync bits (4)

Alarm/Spare (xyxx) bits (4)

Time slot signaling (abcd) bits (120)

Data bits (3840) (bits individually selectable)

This format is intended for clear channel (unchannelized) applications of multiframe E1. Numbering of the data bits for error targeting into a multiframe of this format is detailed in Table K.2.

Frame	Data Bits	Frame	Data Bits	Frame	Data Bits	Frame	Data Bits
0	1-240	4	961-1200	8	1921-2160	12	2881-3120
1	241-480	5	1201-1440	9	2161-2400	13	3121-3360
2	481-720	6	1441-1680	10	2401-2640	14	3361-3600
3	721-960	7	1681-1920	11	2641-2880	15	3601-3840

Table K.2 E1-Multiframed Clear Channel Data Bit Numbering

Targetable Bits in E1-CRC4 No Signaling Format

When set up for the E1-CRC4 no signaling format (G.703(2.048 Mbps) with CRC4 multiframe structure without signaling), errors can be targeted to the following bits in the frame structure:

Bit To Target (Number of targetable bits)

Frame alignment (F) bits (128)

Data time slots (31) (selected by time slots and time slot bit mask)

This format is intended for channelized applications of CRC4 multiframe E1 without signaling.

Targetable Bits in E1-CRC4 with Signaling Format

When set up for the E1-CRC4 with signaling format (G.703 2.048 Mbps) with CRC4 multiframe structure with signaling), errors can be targeted to the following bits in the frame structure:

Bit To Target (Number of targetable bits)

Frame alignment (F) bits (128)

Multiframe sync bits (4)

Alarm/Spare (xyxx) bits (4)

Time slot signaling (abcd) bits (120)

Data time slots (30) (selected by time slots and time slot bit mask)

This format is intended for channelized applications of CRC4 multiframe E1 with time slot-16 signaling.

Targetable Bits in E1-CRC4 Clear Channel Format

When set up for the E1-CRC4 clear channel format (G.703 2.048 Mbps) with CRC4 multiframe structure), errors can be targeted to the following bits in the frame structure:

Bit To Target (Number of targetable bits)

Frame alignment (F) bits (128)

Data bits (3968) (bits individually selectable)

This format is intended for clear channel (unchannelized) applications of CRC4 multiframe E1. Numbering of the data bits for error targeting into a multiframe of this format is detailed in Table K.3.

Frame	Data Bits	Frame	Data Bits	Frame	Data Bits	Frame	Data Bits
0	1-248	4	993-1240	8	1985-2232	12	2977-3224
1	249-496	5	1241-1488	9	2233-2480	13	3225-3472
2	497-744	6	1489-1736	10	2481-2728	14	3473-3720
3	745-992	7	1737-1984	11	2729-2976	15	3721-3968

Table K.3 E1 CRC4 Clear Channel Data Bit Numbering

Targetable Bits in T1-ESF No Signaling Format

When set up for the T1-ESF no signaling format (extended superframe without signaling), errors can be targeted to the following bits in the multiframe structure:

Bit To Target (Number of targetable bits)

Data Link (FDL) bits (12)

Framing Pattern (FPS) bits (6)

Multiframe CRC bits (6)

Data channels (24) (selected by time slots and time slot bit mask)

This format is intended for channelized applications of extended superframe T1 without signaling.

Targetable Bits in T1-ESF with Signaling Format

When set up for the T1-ESF with signaling, errors can be targeted to the following bits in the multiframe structure:

Bit To Target (Number of targetable bits)
Data Link (FDL) bits (12)
Framing Pattern (FPS) bits (6)
Multiframe CRC bits (6)
Signaling bits (ABCD) (96)
Data channels (24) (selected by time slots and time slot bit mask)

This format is intended for channelized applications of extended superframe T1 with signaling.

Targetable Bits in T1-ESF Clear Channel Format

When set up for the T1-ESF clear channel format, errors can be targeted to the following bits in the multiframe structure:

Bit To Target (Number of targetable bits)
Data Link (FDL) bits (12)
Framing Pattern (FPS) bits (6)
Multiframe CRC bits (6)
Data bits (4608) (bits individually selectable)

This format is intended for clear channel (unchannelized) applications of extended superframe T1. Numbering of the data bits for error targeting into a multiframe of this format is detailed in Table K.4.

Frame	Data Bits	Frame	Data Bits	Frame	Data Bits	Frame	Data Bits
1	1-192	7	1153-1344	13	2305-2496	19	3457-3648
2	193-384	8	1345-1536	14	2497-2688	20	3649-3840
3	385-576	9	1537-1728	15	2689-2880	21	3841-4032
4	577-768	10	1729-1920	16	2881-3072	22	4033-4224
5	769-960	11	1921-2112	17	3073-3264	23	4225-4416
6	961-1152	12	2113-2304	18	3265-3456	24	4417-4608

Table K.4 T1 ESF Clear Channel Data Bit Numbering

Targetable Bits in T1-D3/D4 No Signaling Format

When set up for the T1-D3/D4 no signaling format (superframe without signaling), errors can be targeted to the following bits in the multiframe structure:

Bit To Target (Number of targetable bits)

Framing F_T bits (6) (framing pattern)

Multiframing F_S bits (6) (multiframe pattern)

Data channels (24) (selected by time slots and time slot bit mask)

This format is intended for channelized applications of superframe T1-D3/D4 without signaling.

Targetable Bits in T1-D3/D4 with Signaling Format

When set up for the T1-D3/D4 with signaling format, errors can be targeted to the following bits in the multiframe structure:

Bit To Target (Number of targetable bits)

F_T bits (6) (framing pattern)

F_S bits (6) (multiframe pattern)

Signaling bits A, B (48)

Data channels (24) (selected by time slots and time slot bit mask)

This format is intended for channelized applications of superframe T1 D3/D4 with signaling.

Targetable Bits in T1-D3/D4 Clear Channel Format

When set up for the T1-D3/D4 clear channel format, errors can be targeted to the following bits in the multiframe structure:

Bit To Target (Number of targetable bits)

F_T bits (6) (framing pattern)

F_S bits (6) (multiframe pattern)

Data bits (2304) (bits individually selectable)

This format is intended for clear channel (unchannelized) applications of superframe T1. Numbering of the data bits for error targeting into a multiframe of this format is detailed in Table K.5.

Frame Number	Data Bit Numbers	Frame Number	Data Bit Numbers
1	1-192	7	1153-1344
2	193-384	8	1345-1536
3	385-576	9	1537-1728
4	577-768	10	1729-1920
5	769-960	11	1921-2112
6	961-1152	12	2113-2304

Table K.5 T1 D3/D4 Clear Channel Data Bit Numbering

Targeting Error Types Available

The error targeting function provides the following six possible error types that can be targeted to specific places in the formatted data stream. In addition to these error types, any bit can be selected to receive no errors which is displayed as a dash (-) on the selection screen.

The six error types are:

1. **Random Logic error:** This error type is displayed as an 'R' on the SX/12 display. It enables a selected bit position to receive a logic error (bit reversal) when an error event occurs for this particular bit time. Logic errors will occur in this bit position with the probability determined by the random and burst error generators.

2. **Random Space error:** This error type is displayed as an 'S' on the SX/12 display. It enables a selected bit position to be replaced with a space (or zero) bit when an error event generates an error bit for this particular bit time. Random zeros will occur in this bit position with the probability determined by the random and burst error generators.

3. **Random Mark error:** This error type is displayed as an 'M' on the SX/12 display. It enables a selected bit position to be replaced with a mark (or one) bit when an error event occurs for this particular bit time. Random ones will occur in this bit position with the probability determined by the random and burst error generators.

4. **Forced Logic error:** This error type is displayed as an 'E' on the SX/12 display. It enables a selected bit position to receive a logic error (bit reversal) at every occurrence of this selected bit in the data stream. Logic errors will occur in this bit position regardless of the activity of the random or burst error generators.

5. **Forced Space error:** This error type is displayed as a '0' on the SX/12 display. It enables a selected bit position to receive a logic zero at every occurrence of this selected bit in the data stream. Logic zeros will occur in this bit position regardless of the programming of the random or burst error generators.

6. **Forced Mark error:** This error type is displayed as a '1' on the SX/12 display. It enables a selected bit position to receive a logic one at every occurrence of this selected bit in the data stream. Logic ones will occur in this bit position regardless of the programming of the random or burst error generators.

Operation of the Extended T1/E1 Simulation Option

Upon power-up, the prompt

Extended T1/E1 Simulation Module
installed

will be displayed momentarily after the normal SX/12 sign-on message to indicate that the option is present. If the option is already enabled, a help prompt:

Use <SELECT> to toggle between Main and
T1/E1 screens. Press <CLR> to continue.

will be displayed momentarily. The SX/12 then displays the T1/E1 status screen. Pressing the [SELECT] key will alternate the display between the T1/E1 status screen and the SX/12's normal main screen. On the main screen, the T1 or E1 mode indicator will be displayed on the lower left corner to indicate that the option is enabled in either T1 or E1 mode. This T1/E1 indicator has a lower display priority than other indicators that also use that area on the display and is not displayed if one of these mode indicators is on. The higher priority mode indicators are Bypass, Inward Loopback, Outward Loopback and Keyboard Lock.

Enabling/Disabling the Extended T1/E1 Simulation Option

To enable the Extended T1/E1 Simulation Option:

Press the [OPTIONS] key until the prompt

Enter Extended T1/E1 Simulation mode?

appears.

Press the [ENTER] key to enable the option. The help prompt:

Use <SELECT> to toggle between Main and
T1/E1 screens. Press <CLR> to continue.

will be displayed momentarily before returning to the main display. The T1 or E1 mode indicator will be displayed in the lower left corner of the display depending on the current frame format selected.

To disable the option:

Press the [OPTIONS] key until the prompt

Leave Extended T1/E1 Simulation mode?

appears.

Press the [ENTER] key to leave the option. The T1 or E1 mode indicator will no longer be displayed in the lower left corner of the SX/12's main screen.

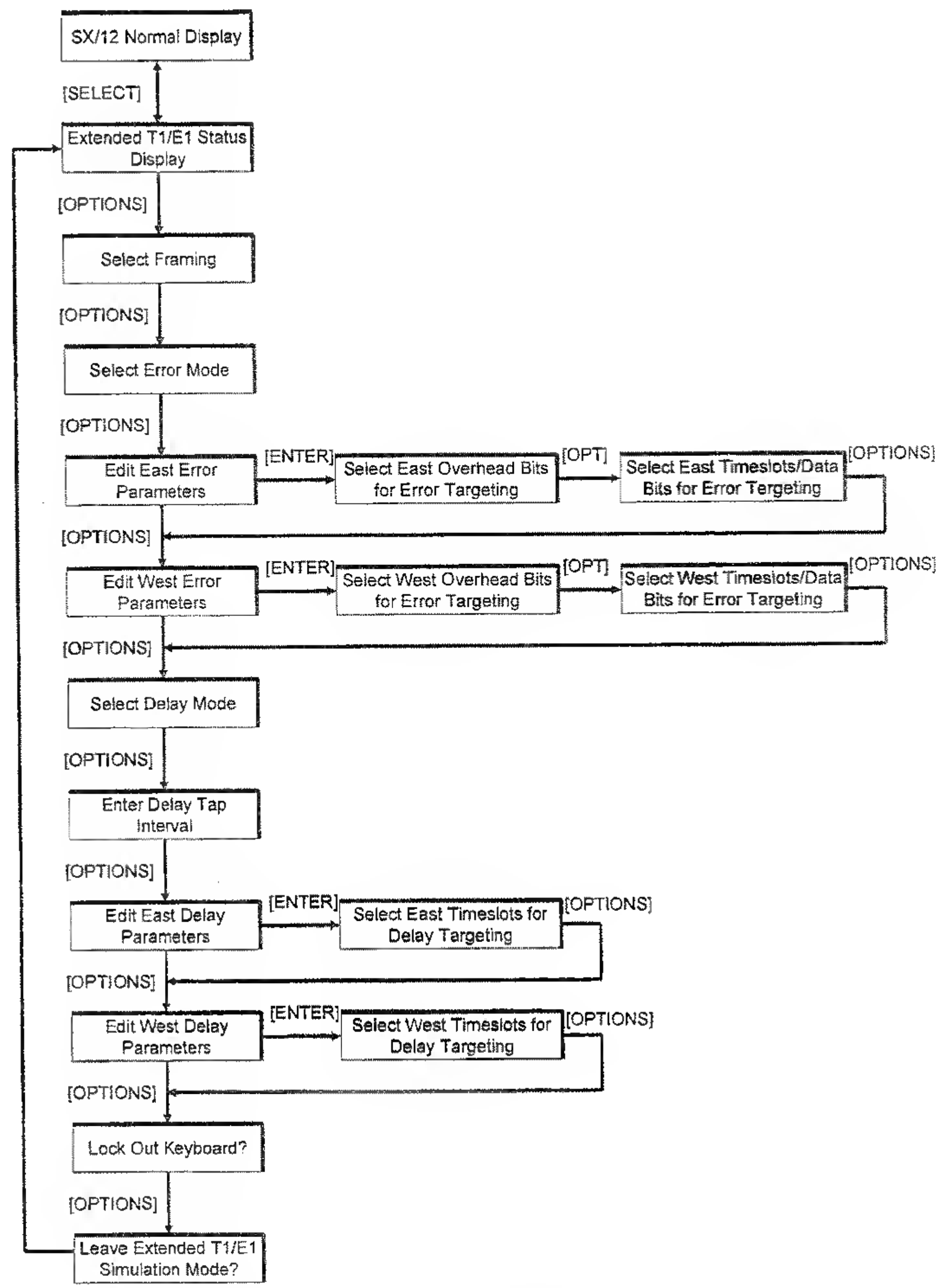

Figure K.1 — Extended T1/E1 Simulation Menu Structure

Extended T1/E1 Status Screen

The [SELECT] key is used to toggle between the SX/12's normal display and the Extended T1/E1 status screen shown below:

```
FRM:ESF    E: C  F  S  D   W:- - - -     NO SYNC | EAST
<OPT>=edit params,<SEL>=return              *SYNC | WEST
```

Extended T1/E1 Simulation status information is provided by this screen. The first field of the display identifies the frame format that is being used. The possible formats displayed are E1-F, E1-Fc, E1-MFs, E1-MFc, CRC4, CRC4s, CRC4c, D3/D4, D3/D4s, D3/D4c, ESF, ESFs, and ESFc. The lower case "s" indicates a format with signaling was chosen while the lower case "c" indicates clear channel (or unchannelized) format. Data bits can be individually targeted rather than time slots when clear channel formats are selected.

Active T1/E1 error and delay settings for the East and West channels are summarized in the second field. Channel designators "E:" and "W:" identify the East and West settings summaries. The active settings indicators are "C" for channel (time slot) errors, "F" for frame bit errors, "S" for signaling bit errors, and "D" for time slot delay. Inactive parameters are indicated with the "-" character.

The third field, located on the right end of the display, indicates whether or not the SX/12 is synchronized to the frames of the data stream. The top line displays the sync status for the East channel, while the bottom line displays the sync status for the West channel. When sync is acquired, "SYNC" is displayed on the respective channel. If sync is lost after the initial acquisition and restored, an "*" is displayed by the sync indicator to indicate the sync loss. Pressing the [CLR] key will reset the sync loss indicator. If sync is not acquired, "NO SYNC" is displayed.

The menu on the bottom of the display serves as a reminder that the [OPTIONS] key is used to enter the Extended T1/E1 menu and the [SELECT] key returns the display to the SX/12 normal screen.

Extended T1/E1 Menu Structure

The Extended T1/E1 menu is entered by pressing the [OPTIONS] key from the Extended T1/E1 status screen. The [OPTIONS] key is used to cycle the display through the prompts of all the Extended T1/E1 options, as shown in Figure K.1 . Pressing the [CLR] key at any of those prompts will return the display back to the Extended T1/E1 status display. At any of the "Edit East Error Parameters?", "Edit West Error Parameters?", "Edit East Delay Parameters?", or "Edit West Delay Parameters?" prompts, pressing the [ENTER] key displays an appropriate menu for that function. Once one of the four menus is displayed, the [OPTIONS] key is used to cycle the display through all of the settable parameters for this function. After stepping through all the parameters for this menu, the display returns to the next item on the main T1/E1 menu.

Pressing the [CLR] key from any parameter screen will return the display back to the Extended T1/E1 status screen. Any changes made on that parameter screen are not entered and are lost. To save all changes, be sure to press the [CLR] key from a parameter screen on which no changes have been made or cycle through all menus with the [OPTIONS] key until the T1/E1 status screen is displayed.

Selecting the Frame Format

To select the desired frame format:

Press the [OPTIONS] key from the T1/E1 status display. The following prompt appears.

Select Framing:___
<SEL>=choose, <OPT>=OK/next, <CLR>=esc

The current frame format will be displayed after the colon. The format choices are as described earlier in this appendix. Press the [SELECT] key until the desired format is displayed, then the [OPTIONS] key to accept and move to the next parameter.

Whenever the frame format is changed, all Extended T1/E1 parameters are reset to their default settings of no errors targeted ("-" displayed) and time slot delays set to the main channel delay tap (tap 1 for Single Group mode or tap 4 for Double Group mode).

Selecting the Error Mode

To select the Extended T1/E1 error mode:

Press the [OPTIONS] key from the Extended T1/E1 status display until the following screens appears.

Select Error Mode:____
<SEL>=choose,<OPT>=OK/next,<CLR>=esc

When the desired screen is displayed, press the [SELECT] key to select the Continuous or Manual Multiframe burst mode.

The Continuous mode injects targeted errors in every multiframe as determined by the targeting selections for each bit. The Manual Multiframe burst mode only targets errors in a multiframe when the burst inject keys [BW], [BW/E], and [BE] are pressed.

Programming the Extended T1/E1 Error Parameters

To program the Extended T1/E1 error parameters:

Press the [OPTIONS] key from the Extended T1/E1 status display until one of the following screens appears:

Edit East Error Parameters?
<ENT>=yes,<OPT>=nxt,<E<>W>=copy frm WEST

Edit West Error Parameters?
<ENT>=yes,<OPT>=nxt,<E<>W>=copy frm EAST

When the desired screen is displayed, press the [ENTER] key to display the first bit selection screen for that function.

The selection screen that appears next depends on which of the above functions is entered and which frame format is selected. The (E)ast or (W)est error parameter screens will display a set of targetable bits along with one of three selectable editing menus that can be selected with the [.] key. The screens typically will look like the following:

FRM BITS(E) ---- ---- ----
<.>=?,Fm#: 1 5 9

The bottom line on this first screen displays the frame numbers associated with the displayed bits. By pressing the [.] key the next menu is displayed:

FRM BITS(E) ---- ---- ----
<.>=?, <0>0,<1>1,<2>E,<3>S,<7>M,<8>R,<9>-

This menu displays the number keys to press to assign one of the error types described earlier to the current bit identified by the cursor. The key assigned to each error type is:

Key	Error Type
[0]	0 (Forced Zero)
[1]	1 (Forced One)
[2]	E (Forced Error)
[3]	S (Random Zero)
[7]	M (Random One)
[8]	R (Random Error)
[9]	- (No Error)

Pressing the [.] key a second time displays the last of the three menus:

FRM BITS(E) ---- ---- ----
<.>=?,<PRV>left,<NXT>right,<OPT>OK/next

This menu displays the keys used to move the cursor to the bit that you wish to assign an error to ([PRV] and [NXT] keys). It also displays the key to use to move to the next T1/E1 parameter screen ([OPTION] key). Pressing the [.] key a third time displays the first of the three menus again. Regardless of which menu is displayed, all of the keys on all three menus are always available.

If all of the bits on a particular bit selection screen cannot be displayed at once, the [PRV] and [NXT] keys are used to access bits not currently displayed by moving the cursor past the end of the currently displayed bits.

For channelized formats, errors are targeted into selected time slots in the frame using the menus just described on the CH ERRS screen. After the time slots (channels) to receive errors are assigned error types, the next field to be set up is a bit mask field which is accessed with the [OPTIONS] key. This field allows you to enable which of the eight bits in the targeted time slots will receive the selected errors. Unselected bits in targeted time slots as well as untargeted time slots do not receive any errors. The bit mask menu appears as follows:

CHANNEL BIT MASK(E) ******
<.>=?, Bit: 1 8

The asterisks indicate that by default all bits of the time slots are enabled to receive any errors that may be targeted to a particular time slot. Any disabled bits would be displayed as a "-". Pressing the [.] key at this point displays several additional menus that indicate which key enables or disables the time slot bits, which keys move the cursor, or the key to press to exit to the next option. The [ERR] key is used to enable or disable the bit at the current cursor position and moves the cursor right to the next bit. The [PREV] or [NEXT] keys permit moving the cursor left or right. Pressing the [OPTION] key completes the entry of the bit mask.

For bit selection screens that are used to target errors into the data area of a multiframe in a clear channel format, the frame number menu is replaced with the following menu:

DATA(E) 0001:-------- -------- --------
<.>=?, <4>goto, <6>copy bits, <CLR>clr all

The data bits on this menu are numbered starting from 1. Data bit 0001 is the first data bit in the multiframe. Framing and overhead bits are not present in the displayed sequence of bits. The data bits are numbered consecutively from number 1 as though the framing and other overhead bits did not exist. See the appropriate clear channel framing format section earlier in this appendix for a list of the data bit numbers for each frame of the multiframe.

The go to, copy bits, and clear all functions permit easier entry of the error types for the many bits in a data field. Each function displays a screen for the user to enter parameters for it.

The other two menus (error menu and cursor menu) are the same as previously described.

When all of the bit error selection screens have been displayed by pressing the [OPTION] key, the display returns to the next parameter in the main T1/E1 menu.

Selecting the Delay Mode

To select the Extended T1/E1 delay mode:

Press the [OPTIONS] key from the Extended T1/E1 status display until the following screen appears:

Select Delay Mode:____
<SEL>=choose,<OPT>=OK/next,<CLR>=esc

When the desired screen is displayed, press the [SELECT] key to select the Single Group or Double Group mode.

The modes provide two possible delay tap assignments as defined in the table at the beginning of the appendix.

Selecting the Delay Tap Interval

To select the Extended T1/E1 delay tap interval:

Press the [OPTIONS] key from the Extended T1/E1 status display until the following screens appears.

Select Delay Tap Interval(ms): 0001
<SEL>=units,<OPT>=OK/next,<CLR>=esc

When the desired screen is displayed, press the [SELECT] key to select the desired units of milliseconds or frames, then enter the desired tap interval value. Milliseconds can range from one to 16, while frames can range from one to 128. Follow the entry with the [ENTER] key to accept it. The use of this parameter is defined in the delay table at the beginning of the appendix.

Programming the Extended T1/E1 Delay Parameters

To program the Extended T1/E1 delay parameters:

Press the [OPTIONS] key from the Extended T1/E1 status display until one of the following screens appears:

Edit East Delay Parameters?
<ENT>=yes,<OPT>=nxt,<E<>W>=copy frm WEST

Edit West Delay Parameters?
<ENT>=yes,<OPT>=nxt,<E<>W>=copy frm EAST

When the desired screen is displayed, press the [ENTER] key to display the edit screen for that direction.

```
CHAN DLY(E)  1111 1111 1111 2222 5555 ----
<,>=?        1    5    9    13   17   21
```

This parameter screen determines which time slots (channels) in the T1/E1 frame will be delayed and by how much. The amount of delay is determined by the delay tap number assigned to each time slot, the delay mode, the delay tap interval, and the main channel

delay settings. The time slot delay assignments are indicated by a number from 0 to 9 which are defined in Table K.1 at the beginning of this appendix. The time slot numbers are displayed on this initial menu. The default delay tap assignment is all time slots assigned to the main channel delay (delay tap 1 for the Single Group mode, delay tap 4 for the Double Group mode).

There are six additional menus accessed with the [.] key that define the keys used to assign the delay taps and the cursor movement keys. The cursor movement menu is displayed next by pressing the [.] key:

CHAN DLY(E) 1 1 1 1 1 1 1 1 1 1 1 1 2 2 2 2 5 5 5 5 ----
<.>=?,<PRV>left,<NXT>right,<OPT>OK/next

This menu indicates the keys used to move the cursor to the time slot that you wish to assign a delay tap to ([PRV] and [NXT] keys). It also displays the key to use to move to the next T1/E1 parameter screen ([OPTION] key). Since all of the time slots cannot be displayed at once, the [PRV] and [NXT] keys are used to access time slots not currently displayed by moving the cursor past the end of the currently displayed time slots. Pressing the [.] key for the third time displays the first delay tap menu:

CHAN DLY(E) 1 1 1 1 1 1 1 1 1 1 1 1 2 2 2 2 5 5 5 5 ----
<.>=?,<0>0000ms, <1> 300ms

Each of these five menus displays two of the available delay tap keys. They are displayed by repeatedly pressing the [.] key. All keys on all seven menus are always available regardless of which of the menus is currently displayed. When all of the delay taps have been assigned, move to the next parameter by pressing the [OPTION] key.

Operational Details of the Extended T1/E1 Simulation Option

Due to the complex nature of the simulation capabilities of this option, there are a few things that should be kept in mind regarding the details of its operation. They are:

1. When the current frame format is changed, all error targeting and delay targeting parameters are set to their default values. No bits are targeted to receive errors and all time slots are set to receive the delay tap corresponding to the main channel delay (delay tap 1 for the Single Group mode, delay tap 4 for the Double Group mode). This reprogramming of the settings may cause a temporary discontinuity in the data stream.

2. When any of the error targeting parameters are changed, the error targeting function is briefly shut off and the time slot delays temporarily receive the the main channel delay while the option's circuitry is being reprogrammed. As soon as that is complete, error targeting and delay targeting resume with the new settings. As a result, if any of the time slots are programmed to receive a delay other than the main channel delay, a temporary discontinuity occurs in the data stream while the circuitry is being reprogrammed. It is recommended that if you are not using time slot delays, you should set all of the time slots to the delay tap corresponding to the main channel delay (the default setting). If no delay is desired, just set the main channel delay to zero.

3. When the delay targeting parameters are changed, a temporary discontinuity occurs in the data stream while the delay circuitry is being reprogrammed.

4. After the option is enabled, but before sync is first achieved, errors and the main channel delay are applied to the entire data stream as if the option were not enabled. Once sync is achieved, errors and delay are then applied to only targeted locations. If sync is lost, the option continues to target errors and delay based on the last frame alignment that it had until a new frame alignment is achieved. This could briefly cause errors and delay to oc-

cur in untargeted locations if there was actually a discontinuity in the data stream which caused the sync loss.

Keyboard Lock out

The keyboard on the SX/12 can be disabled to prevent accidental modifications of the parameters once it has been set up. This option allows the user to lock out the keyboard with the Extended T1/E1 status screen displayed. The [OPTIONS], [CLR], [BW], [BW/E] and [BE] keys will continue to function. The [OPTIONS] key is used to unlock the keyboard. The [CLR] key is used to reset the sync loss indicator and the [BW], [BW/E] and [BE] keys are used to trigger manual burst errors or manual multiframe bursts. To lock out the keyboard:

Press the [OPTIONS] key from the Extended T1 status display until the following prompt appears.

Lock out keyboard?
<ENTER> for yes, <OPTIONS> for next optn

Press the [ENTER] key to accept. The display will now be locked on the Extended T1/E1 status display.

To unlock the keyboard:

Press the [OPTIONS] key to make the following prompt appear:

Unlock keyboard?
<ENTER> for yes, <CLR> to exit

Press the [ENTER] key to unlock the keyboard.

Exiting Extended T1/E1 Simulation Mode

To leave the extended T1/E1 simulation mode:

Press the [OPTIONS] key from the Extended T1/E1 status display until the following prompt appears.

Leave Extended T1/E1 Simulation mode?
<ENTER> for yes, <OPTIONS> for next optn

Press the [ENTER] key to exit the T1/E1 mode. The display will return to the main SX/12 parameter display. To stay in the T1/E1 mode, press the [OPTION] key instead.

Remote Control of the Extended T1/E1 Simulation Option

The current revision of the extended T1/E1 simulation option software does not provide support for remote control of these functions. Remote control support will be included in the next software release. Please contact the factory for current availability of this software update.

Appendix L
RS-423-A (RS-449) Interface

Description

The RS-423-A interface module is designed to convert between the TTL signals used within the SX/12 and signals complying with the EIA Standard RS-423-A. East and West female "D" type connectors are provided for connecting to Data Terminal Equipment. A male "D" type connector is also provided for applications requiring hookup to Data Communications Equipment. Only a single West connector is used at a time. The active connector is selected by the DCE/DTE selection switch on the rear panel of the SX/12. The RS-423-A interface can operate with either DTE or DCE-provided transmit timing. The selection of the transmit timing mode is made with the EXTERNAL TRANSMIT TIMING switch on the rear panel of the SX/12.

This interface installs in the SX/12 interface plug-in opening on the rear panel using the internal flat cable provided.

Specifications

Maximum signalling rate - 100 Kb/s

Data Polarity -	Function OFF; Signal Condition Mark; Binary "1"; Interchange voltage < -3.6V Function ON; Signal Condition Space; Binary "0"; Interchange voltage > 3.6V
Drivers-	Signal swing; Unbalanced ±3.6V minimum into 450 ohms
Receivers -	Balanced differential; Load Impedance ≥4000 ohms
Data timing -	Data received by the SX/12 is sampled on the ON to OFF transition of the timing signal. Data transmitted by the SX/12 is clocked on the OFF to ON transition of the timing signal.
Cabling -	Less than 200 feet recommended, signal return lead required for each active input

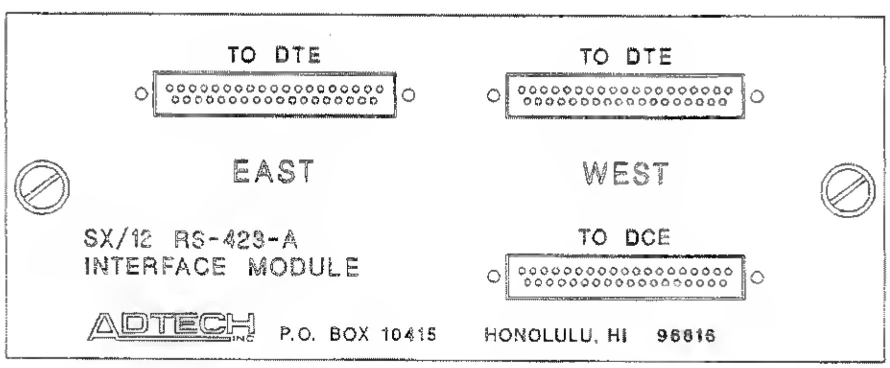

Figure L.1 RS-423-A Interface

Signalling Leads

DTE - DTE Configuration

East/West Connector:	CTS and RTS are connected together at each connector DM and RR are held "on"

DTE - DCE Configuration, delay > 0

East Connector:	CTS and RTS are connected together DM and RR are held "on"
West Connector:	RTS and TR are held "on"

DTE - DCE Configuration, delay = 0

East/West Connector:	CTS (East) connected to CTS (West) RTS (East) connected to RTS (West) DM (East) connected to DM (West) TR (East) connected to TR (West)

Connector Pin Assignments

East "to DTE" Connector

Pin	Circuit	Signal	Lead Status
1	SHIELD	Protectiva Ground	Strapped to interface panel
2	SI	Signaling Rate Indicator	Output (Internally forced on)
4,22	SD(A,B)	Send Data	West channel data input
5,23	ST(A,B)	Send Timing	Output
6,24	RD(A,B)	Receive Data	East channel data output
7,25	RS(A,B)	Request to Send	Input
8,26	RT(A,B)	Receive Timing	Output
9,27	CS(A,B)	Clear to Send	Output
11,29	DM(A,B)	Data Mode	Output
12,30	TR(A,B)	Terminal Ready	Input
13,31	RR(A,B)	Receiver Ready	Output (Internally forced on)
15	IC	Incoming Call	Output (Internally forced off)
17,35	TT(A,B)	Terminal Timing	Input
18	Tm	Test Mode	Output (Internally forced off)
19	SG	Signal Ground	Internally connected to circuit ground
20	RC	Receive Common	Internally connected to circuit ground
33	SQ	Signal Quality	Output (Internally forced on)
36	SB	Standby Indicator	Output (Internally forced off)
37	SC	Send Common	Internally connected to circuit ground

Connector Pin Assignment

West "to DTE" Connector

Pin	Circuit	Signal	Lead Status
1	SHIELD	Protective Ground	Strapped to Interface panel
2	SI	Signaling Rate Indicator	Output (Internally forced on)
4,22	SD(A,B)	Send Data	East channel data input
5,23	ST(A,B)	Send Timing	Output
6,24	RD(A,B)	Receive Data	West channel data output
7,25	RS(A,B)	Request to Send	Input (Internally looped to CS)
8,26	RT(A,B)	Receive Timing	Output
9,27	CS(A,B)	Clear to Send	Output (Internally looped to RS)
11,29	DM(A,B)	Data Mode	Output (Internally forced on)
12,30	TR(A,B)	Terminal Ready	Open
13,31	RR(A,B)	Receiver Ready	Output (Internally forced on)
15	IC	Incoming Call	Output (Internally forced off)
17,35	TT(A,B)	Terminal Timing	Input
18	Tm	Test Mode	Output (Internally forced off)
19	SG	Signal Ground	Internally connected to circuit ground
20	RC	Receive Common	Internally connected to circuit ground
33	SQ	Signal Quality	Output (Internally forced on)
36	SB	Standby Indicator	Output (Internally forced off)
37	SC	Send Common	Internally connected to circuit ground

Connector Pin Assignments

West "to DCE" Connector

Pin	Circuit	Signal	Lead Status
1	SHIELD	Protective Ground	Strapped to interface panel
2	SI	Signaling Rate Indicator	Open
4,22	SD(A,B)	Send Data	West channel data output
5,23	ST(A,B)	Send Timing	Input
6,24	RD(A,B)	Receive Data	East channel data input
7,25	RS(A,B)	Request to Send	Output
8,26	RT(A,B)	Receive Timing	Input
9,27	CS(A,B)	Clear to Send	Input
10	LL	Local Loopback	Output (Internally forced off)
11,29	DM(A,B)	Data Mode	Input
12,30	TR(A,B)	Terminal Ready	Output
13,31	RR(A,B)	Receiver Ready	Open
15	IC	Incoming Call	Open
16	SF/SR	Select Frequency/ Signalling Rate Indicator	Output (Internally forced on)
17,35	TT(A,B)	Terminal Timing	Output
18	TM	Test Mode	Open
19	SG	Signal Ground	Internally connected to circuit ground
20	RC	Receive Common	Internally connected to circuit ground
28	IS	Terminal in Service	Output (Internally forced on)
32	SS	Select Standby	Output (Internally forced off)
33	SQ	Signal Quality	Open
34	NS	New Signal	Output (Internally forced off)
36	SB	Standby Indicator	Open
37	SC	Send Common	Internally connected to circuit ground

RS-423-A INTERFACE

Appendix M

MIL-STD-188-114 Interface

Description

The MIL-STD-188-114 interface module is designed to convert between the TTL signals used within the SX/12 and signals complying with MIL Standard 188-114 for balanced signals. East and West female "D" type connectors are provided for connecting to Data Terminal Equipment. A male "D" type connector is also provided for applications requiring hookup to Data Communications Equipment. Only a single West connector is used at a time. The active connector is selected by the DCE/DTE selection switch on the rear panel of the SX/12. The MIL-STD-188-114 interface can operate with either DTE or DCE-provided transmit timing. The selection of the transmit timing mode is made with the EXTERNAL TRANSMIT TIMING switch on the rear panel of the SX/12.

This interface installs in the SX/12 interface plug-in opening on the rear panel using the internal flat cable provided.

Specifications

Maximum signalling rate - 2.048 Mb/s

Data Polarity -	Function OFF; Signal Condition Mark; Binary "1"; Line A negative relative to line B Function ON; Signal Condition Space; Binary "0"; Line A positive relative to line B
Drivers-	Signal swing for line A and B; Balanced ±2V minimum, ±3V maximum into open circuit
Receivers -	Balanced differential; Load Impedance: ≥4000 ohms, 100 ohm terminator optional
Data timing -	Data received by the SX/12 is sampled on the ON to OFF transition of the timing signal. Data transmitted by the SX/12 is clocked on the OFF to ON transition of the timing signal.
Cabling -	Less than 200 feet recommended

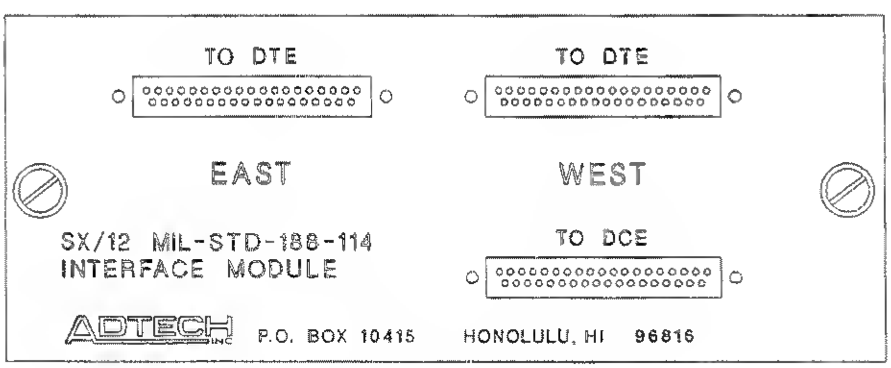

Figure M.1 MIL-STD-188-114 Interface

Signalling Leads

DTE - DTE Configuration

East/West Connector: CTS and RTS are connected together at each connector

DTE - DCE Configuration, delay > 0

East Connector: CTS and RTS are connected together

West Connector: RTS and DTR are held "on"

DTE - DCE Configuration, delay = 0

East/West Connector: CTS (East) connected to CTS (West)
RTS (East) connected to RTS (West)
DTR (East) connected to DTR (West)

Connector Pin Assignments

East "to DTE" Connector

Pin	Circuit	Signal	Lead Status
1	SHIELD	Protective Ground	Strapped to interface panel
4,22	SD(A,B)	Send Data	West channel data input
5,23	ST(A,B)	Send Timing	Output
6,24	RD(A,B)	Receive Data	East channel data output
7,25	RTS(A,B)	Request to Send	Input
8,26	RT(A,B)	Receive Timing	Output
9,27	CTS(A,B)	Clear to Send	Output
12,30	DTR(A,B)	Data Terminal Ready	Input
17,35	TT(A,B)	Terminal Timing	Input
19	SG	Signal Ground	Internally connected to circuit ground
20	RC	Receive Common	Internally connected to circuit ground
37	SC	Send Common	Internally connected to circuit ground

West "to DTE" Connector

Pin	Circuit	Signal	Lead Status
1	SHIELD	Protective Ground	Strapped to interface panel
4,22	SD(A,B)	Send Data	East channel data input
5,23	ST(A,B)	Send Timing	Output
6,24	RD(A,B)	Receive Data	West channel data output
7,25	RTS(A,B)	Request to Send	Input (Internally looped to CTS)
8,26	RT(A,B)	Receive Timing	Output
9,27	CTS(A,B)	Clear to Send	Output (internally looped to RS)
17,35	TT(A,B)	Terminal Timing	Input
19	SG	Signal Ground	Internally connected to circuit ground
20	RC	Receive Common	Internally connected to circuit ground
37	SC	Send Common	Internally connected to circuit ground

West "to DCE" Connector

Pin	Circuit	Signal	Lead Status
1	SHIELD	Protective Ground	Strapped to interface panel
4,22	SD(A,B)	Send Data	West channel data output
5,23	ST(A,B)	Send Timing	Input
6,24	RD(A,B)	Receive Data	East channel data input
7,25	RTS(A,B)	Request to Send	Output
8,26	RT(A,B)	Receive Timing	Input
9,27	CTS(A,B)	Clear to Send	Input
12,30	DTR(A,B)	Data Terminal Ready	Output
17,35	TT(A,B)	Terminal Timing	Output
19	SG	Signal Ground	Internally connected to circuit ground
20	RC	Receive Common	Internally connected to circuit ground
37	SC	Send Common	Internally connected to circuit ground

Appendix N

Conditioned Diphase Interface

Introduction

The Conditioned Diphase Interface module is designed to convert between the NRZ TTL signals used within the SX/12 and 1200 bps to 32,000 bps digital signals in the conditioned diphase format. The electrical signals at the conditioned diphase interface are MIL-STD-188-114 balanced signals. East and West dual banana jacks are provided for receive and transmit data. Another banana jack is provided as a ground reference point and should be connected to the external equipment's ground reference. LED indicators provide line status information. A BNC type connector provides a TTL-level clock source of the selected data rate from the SX/12's frequency synthesizer. The interface installs in the interface opening on the rear panel using the internal flat cable provided.

The Conditioned Diphase Interface module has the following capabilities:

- Operates at conditioned diphase bit rates of 1200, 2400, 4800, 9600, 16000, and 32000 bps
- Signal level is MIL-STD-188-114 balanced electrical levels.
- Interface is transparent to data framing.
- Interfaces with military network and terminal equipment.

Transmit Timing Mode

The Conditioned Diphase interface will operate with the SX/12 in several transmit timing modes. Available transmit timing sources include: Recovered Receive clock, SX/12 Internal clock, and External clock.

Recovered Receive clock is the clock recovered from the receive data. This would be used as the transmit timing source if the equipment connected to the SX/12 is providing the master timing. In this case, the SX/12 will use recovered receive clock to transmit data out the other end of the simulated channel.

Internal clock is the clock generated by the SX/12. This would be used as the transmit timing source if the equipment connected to the SX/12 is operating with loop timing. In this case the SX/12 is the source of master network timing.

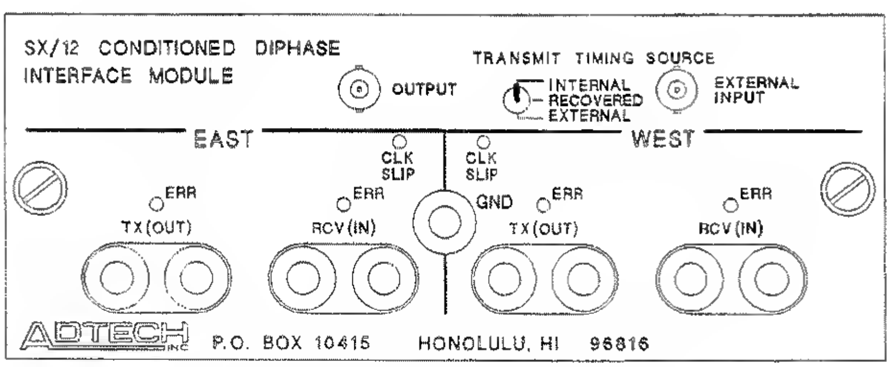

Figure N.1 Conditioned Diphase Interface

CONDITIONED DIPHASE INTERFACE

External clock is a clock source connected to the Conditioned Diphase Interface's EXTERNAL INPUT. This would be used if the equipment connected to the SX/12 is operating with loop timing. In this case, the external clock source is the source of master network timing. This clock source could include jitter, wander, and frequency error to further stress the equipment under test's receive interface and clock recovery circuits.

Regardless of which transmit timing source is selected, the SX/12 requires that its data rate parameter be set to one of the available rates of 1200, 2400, 4800, 9600, 16000, or 32000 Hz (bps) and the External Transmit Timing switch be set to ON for proper operation of the SX/12 with this interface. The diphase interface also must be set to operate at the same rate as that set as the SX/12 data rate parameter by properly positioning the movable shorting jumper on the bottom circuit board of the interface to the desired rate. Once these settings have been made and the transmit clocking mode selected, the conditioned diphase interface is ready for use.

Specifications

TX, RX Connectors:
Dual banana jacks

Signal Format:
Conditioned diphase signal in MIL-STD-188-114 balanced electrical levels

Data Rate:
1200, 2400, 4800, 9600, 16000, 32000 bps

Data Format:
Interface is transparent to data framing

Output Drivers:
Signal swing for line A and B; Balanced ±2V minimum, ±3V maximum into open circuit

Input Receivers:
Balanced differential; Load Impedance: ≥4000 ohms, 100 ohm terminator optional

Data timing:
Self-clocking conditioned diphase format

Transmit timing modes:
Internal, External, and Recovered

Elastic Buffer:
256 bit input elastic buffer handles short term loop timing clock variations for Internal and External clock modes

Clock Generator Output:
TTL level into 75 ohms, BNC female connector

External Clock Input:
TTL level into 75 ohms, BNC female connector

Cabling:
Less than 200 feet recommended

Interface Panel Indicators:

CLK SLIP - Indicates the input elastic buffer has overflowed or underflowed due to a clocking problem. The SX/12 data rate and the external equipment data rate do not agree. This is usually caused by a clocking mode or clock rate setup problem.

ERR - Error is lit if the conditioned diphase decoder is unable to properly decode/encode the conditioned diphase signal.

Appendix O

EIA-530 Interface

Description

The EIA-530 interface module is designed to convert between the TTL signals used within the SX/12 and signals complying with the EIA Standard interface EIA-530. East and West female 'D' type connectors are provided for connecting to Data Terminal Equipments (DTE). A male 'D' type connector is also provided for applications requiring hookup to Data Communications Equipment (DCE). Only a single West connector is used at a time and is selected by the DCE/DTE switch located on the rear panel of the SX/12.

Specifications

Maximum data rate - 10 Mb/s	
Data Polarity -	Function OFF; Signal Condition Mark; Binary "1"; Line A is more negative than line B Function ON; Signal Condition Space; Binary "0"; Line A is more positive than line B.
Drivers-	Signal swing; Balanced differential ±5 volts peak-to-peak into 100 ohms; RS-422-A levels
Receivers -	Load Impedance; 220 ohms; RS-422-A levels
Data timing -	Data received by the SX/12 is sampled on the ON to OFF transition of the timing signal. Data transmitted by the SX/12 is clocked on the OFF to ON transition of the timing signal.
Cabling -	Less than 200 feet recommended

Jumper Options

Because data and clock signals do not travel exactly the same paths in the SX/12 and the outside world, the phase relationship between the data and clock signals can change as they travel along their circuits. At high speeds this phase change can be significant. Located on the interface module circuit board is a pair of jumper option blocks that allow the user to reclock the data. Selecting 'yes' to this option reduces the output clock to output data skew from 60 ns to approximately 10 ns. For the 'to DTE' connectors, this affects the Receiver

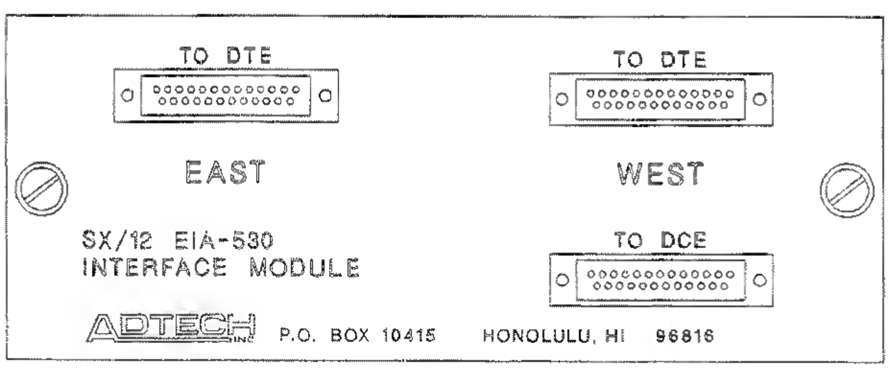

Figure O.1 EIA-530 Interface

Timing (DD) to Received Data (BB) skew. For the West 'to DCE' connector, if the EXTERNAL TRANSMIT TIMING switch is 'off', then the DCE Transmit Timing (DB) to Transmitted Data (BA) skew is affected. If the EXTERNAL TRANSMIT TIMING switch is 'on', then the DTE Transmit Timing (DA) to Transmitted Data (BA) skew is affected. Selecting 'yes' to this option adds a one bit delay which may not be desirable at low data rates.

Facing the back of the interface module, the reclocking options are located below and to the right of the 50 pin flat cable connector. The Reclock East Data Out option is selected with the right jumper block. The Reclock West Data Out option is selected with the left jumper block.

Signalling Leads

DTE - DTE Configuration

East/West Connector:	Request To Send (CA) and Clear To Send(CB) are connected together at each connector DCE Ready (CC) and Received Line Signal Detector (CF) are held 'on'

DTE - DCE Configuration, delay > 0

East Connector:	Request To Send (CA) and Clear To Send(CB) are connected together DCE Ready (CC) and Received Line Signal Detector (CF) are held 'on'
West Connector:	Request To Send (CA) and DTE Ready (CD) are held 'on'

DTE - DCE Configuration, delay = 0

East/West Connector:	Clear To Send(CB) (East) connected to Clear To Send(CB) (West) Request To Send (CA) (East) connected to Request To Send (CA) (West) DCE Ready (CC) (East) connected to DCE Ready (CC) (West) DTE Ready (CD) (East) connected to DTE Ready (CD) (West)

Connector Pin Assignments

East "to DTE" Connector

Pin	Circuit	Signal	Lead Status
1	SHIELD	Protective Ground	Strapped to chassis ground
2,14	BA(A,B)	Transmitted Data	West channel data input
15,12	DB(A,B)	DCE Transmit Timing	Output
3,16	BB(A,B)	Received Data	East channel data output
4,19	CA(A,B)	Request to Send	Input
17,9	DD(A,B)	Receiver Timing	Output
5,13	CB(A,B)	Clear to Send	Output
6,22	CC(A,B)	DCE Ready	Output
20,23	CD(A,B)	DTE Ready	Input
8,10	CF(A,B)	Received Line Signal Detector	Output
24,11	DA(A,B)	DTE Transmit Timing	Input
25	TM	Test Mode	Output (Internally forced off)
18	LL	Local Loppback	No connection
21	RL	Remote Loopback	No connection
7	AB	Signal Ground	Internally connected to circuit ground

West "to DTE" Connector

Pin	Circuit	Signal	Lead Status
1	SHIELD	Protective Ground	Strapped to chassis ground
2,14	BA(A,B)	Transmitted Data	East channel data input
15,12	DB(A,B)	DCE Transmit Timing	Output
3,16	BB(A,B)	Received Data	West channel data output
4,19	CA(A,B)	Request to Send	Input
17,9	DD(A,B)	Receiver Timing	Output
5,13	CB(A,B)	Clear to Send	Output
6,22	CC(A,B)	DCE Ready	Output
20,23	CD(A,B)	DTE Ready	Input
8,10	CF(A,B)	Received Line Signal Detector	Output
24,11	DA(A,B)	DTE Transmit Timing	Input
25	TM	Test Mode	Output (Internally forced off)
18	LL	Local Loppback	No connection
21	RL	Remote Loopback	No connection
7	AB	Signal Ground	Internally connected to circuit ground

Connector Pin Assignments

West "to DCE" Connector

Pin	Circuit	Signal	Lead Status
1	SHIELD	Protective Ground	Strapped to chassis ground
2,14	BA(A,B)	Transmitted Data	West channel data output
15,12	DB(A,B)	DCE Transmit Timing	Input
3,16	BB(A,B)	Received Data	East channel data input
4,19	CA(A,B)	Request to Send	Output
17,9	DD(A,B)	Receiver Timing	Input
5,13	CB(A,B)	Clear to Send	Input
6,22	CC(A,B)	DCE Ready	Input
20,23	CD(A,B)	DTE Ready	Output
8,10	CF(A,B)	Received Line Signal Detector	No Connection
24,11	DA(A,B)	DTE Transmit Timing	Output
25	TM	Test Mode	No Connection
18	LL	Local Loopback	Output (Internally forced off)
21	RL	Remote Loopback	Output (Internally forced off)
7	AB	Signal Ground	Internally connected to circuit ground

JT2 (6312 kbps) Multi-clock Interface

Description

The JT2 Multi-clock Interface Module is designed to convert between the TTL signals used within the SX/12 and signals complying with CCITT specification for 6.312 MHz T2 signals. BNC connectors are provided for East and West receive and transmit data. LED indicators provide line status information. A BNC connector provides a TTL level 6.312 MHz clock source, while another BNC connector allows an external TTL level clock source to be used as a network clock. A transmit timing selector switch allows the SX/12 to be used in one of three different network timing configurations.

The JT2 Multi-clock Interface Module has the following capabilities:

- Transmit and receive data is B8ZS encoded.
- Transmit pulse shape meets NTT Technical Reference for High Speed Digital Leased Circuit Services.
- Receiver sensitivity is adjustable for 0-4.1 dB or 2.5-6.5 dB cable loss.
- Receiver jitter tolerance meets or exceeds CCITT recommendation G.824; 5 UI, 10 Hz to 50 Hz; 0.1 UI, 2.5 kHz to 60 kHz.
- Interface is transparent to T2 framing.
- Interfaces with network equipment.
- Interfaces with Customer Premises Equipment.
- Three transmit timing modes for timing the T2 transmissions.
- Elastic buffer, size: 256 bits.

Timing Configurations

Three transmit timing modes are selectable with the "TRANSMIT TIMING SOURCE" switch. These are Recovered Timing, Internal Timing and External Timing. The "CLK SLIP" indicator lights if a timing problem is detected, suggesting that an improper timing mode has been selected.

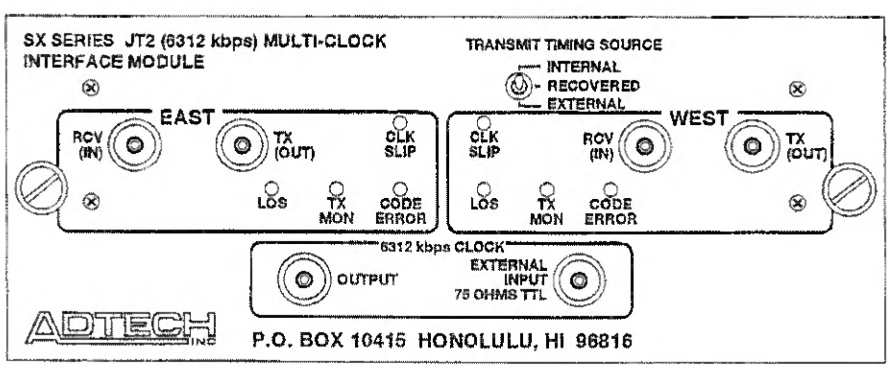

Figure P.1 JT2 Multi-clock Interface

The Recovered Timing mode uses the clock recovered from the received data to time the data transmitted out of the SX/12. In this mode, the master clock is located in the external T2 equipment transmitting to the SX/12. Figure P.2 is a block diagram of this mode.

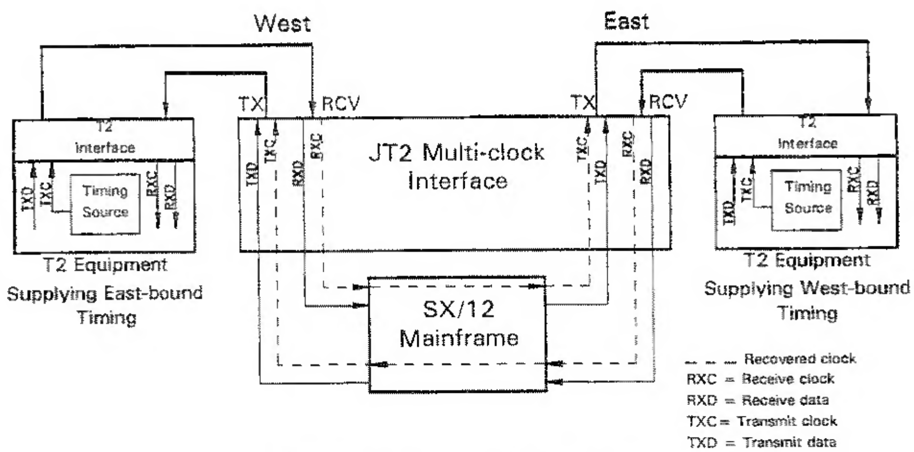

Figure P.2 Recovered Timing Mode

The Internal and External Timing modes allow the SX/12 to become the source of the master clock. The Internal Timing mode uses a highly accurate 6.312 MHz crystal oscillator located on the interface module as the master clock for East and West bound data. Figure P.3 is a block diagram of the Internal Timing mode.

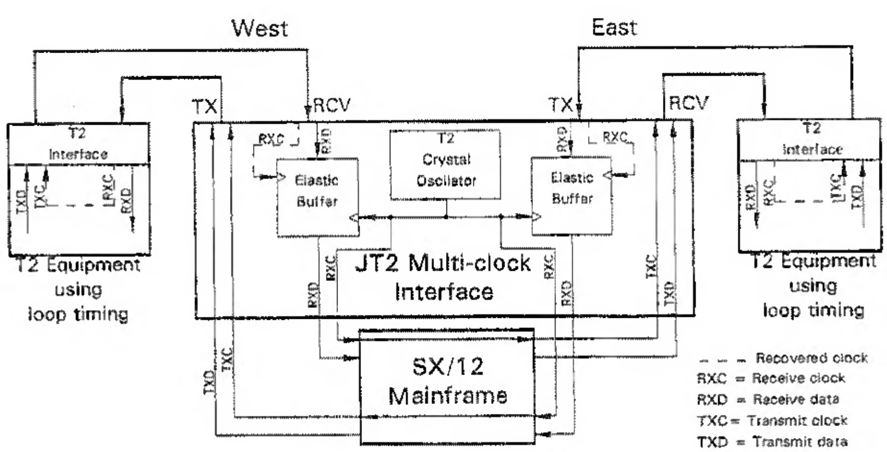

Figure P.3 Internal Timing Mode

The External Timing mode uses an external 6.312 MHz TTL (75 ohms) clock signal provided by the user as the master clock. This mode allows wander, jitter, and clock frequency errors to be injected by the external clock generator. It also allows multiple SX/12s to run off a single master clock. Figure P.4 is a block diagram of this mode.

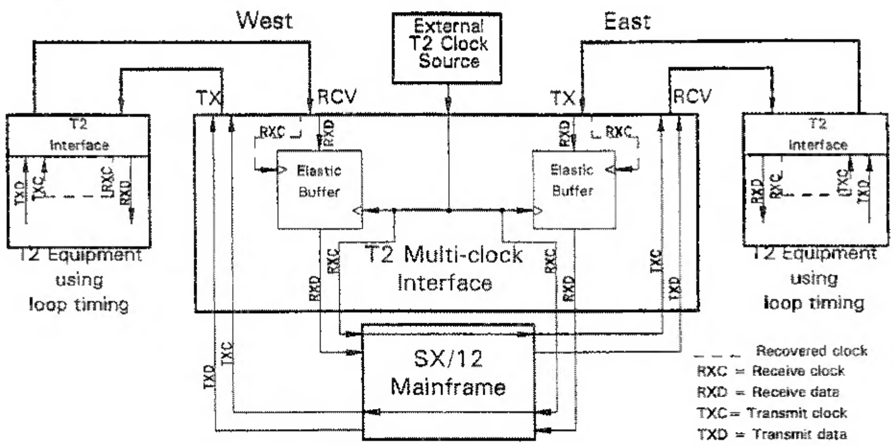

Figure P.4 External Timing Mode

You can choose one of these three modes with the three-position switch labeled "TRANSMIT TIMING SOURCE" on the interface module.

Operation

IMPORTANT: The JT2 interface will only operate when the SX/12 External Transmit Timing Switch is in the "on" position.

The data rate on the SX/12 should be set to 6.312 MHz. If the CLK SLIP indicator comes on during operation, there is a problem with the transmit or receive timing causing the interface's elastic buffer to overflow or underflow. Check that the SX/12's External Transmit Timing switch is in the ON position if this occurs. Also check that all external equipment timing modes are set properly for the transmit timing source selected on the interface. Select the proper line equalization using the dip switch located on the underside of the JT2 Multiclock Interface module.

Dip Switch

This dip switch sets line equalization and testing options for the East and West channels.

Switch Position	Description	Default Settings
1	East Transmit All Ones	off
2	East Local Loopback	off
3	East Remote Loopback	off
4	East Receiver Equalization	off
5	(not used)	n/u
6	West Transmit All Ones	off
7	West Local Loopback	off
8	West Remote Loopback	off
9	West Receiver Equalization	off
10	(not used)	n/u

Transmit All Ones - Setting to "on" causes continuous ones to be transmitted. Used for testing only.
Local Loopback - Setting to "on" routes the transmit data from the SX/12 back into the SX/12 on the same port. Data also goes out the "TX" connector of that port. Used for testing only.
Remote Loopback - Setting to a "on" routes data coming in the "RCV" connector to the "TX" connector of the same port. Used for testing only.
Receiver Equalization - Setting to "off" lets the receiver handle 0 to 4.1 dB of cable loss. Setting to "on" lets the receiver handle 2.5 to 6.5 dB of cable loss.

Specifications

Transmitter:
- Output pulse amplitude: 1.7 - 2.3 Vpk (2.0 Vpk nominal).
- Coding: B8ZS
- Complies with Japanese NTT Technical Reference for High Speed Digital Leased Circuits

Receiver:
- Coding: B8ZS
- Allowable Consecutive Zeros before LOS: 20 - 32. Recovery occurs when receive signal returns.
- Jitter tolerance: Meets or exceeds CCITT recommendation G.824; 5 UI, 10 Hz to 50 Hz; 0.1 UI, 2.5 kHz to 60 kHz.
- Jitter Transfer: 0 dB.
- Input impedance: 75 ohms.
- Transparent to framing.

Clock Generator Output:
- Connector: BNC female.
- Voltage: TTL level into 50 ohms.
- Frequency: 6.312 MHz ±25 ppm
- Duty Cycle: 50%

External Clock Input:
- Connector: BNC female.
- Voltage: TTL levels
- Impedance: 75 ohms.
- Frequency: 6.312 MHz (jitter and frequency error can be added).
- Duty Cycle: 45 - 55% at 1.4 V.

TX, RX Connector:
- BNC female.

Interface Panel Indicators:

LOS - Loss Of Signal is lit when 20 to 32 consecutive zeros have been received. Indicator goes off when receive signal returns.

TX MON - Transmitter Monitor is lit if no signal is present on the TX connector for 20 to 32 consecutive clock cycles.

CODE ERROR - Code Error is lit if a violation of the B8ZS line coding scheme is detected.

CLK SLIP - Clock Slip is lit when the Elastic Buffer overflows or underflows. This will occur when the clocked data on the RCV line is not at the same nominal frequency as the internal or external source clock.